13.8 A 194nW Energy-Performance-Aware IoT SoC Employing a 5.2nW 92.6% Peak Efficiency Power Management Unit for System Performance Scaling, Fast DVFS and Energy Minimization

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A self-powered IoT system-on-chip (SoC) reduces power to sub-μW and employs multiple power-management techniques to trade-off ultra-low power (ULP), higher performance, smaller energy harvester footprint, and longer operating lifetime. Minimum Energy Point Tracking (MEPT) [1-4] keeps an SoC operating at the minimum energy point (MEP) to enhance system lifetime. Previous sample-and-hold MEPT schemes need frequent voltage comparisons and a high-frequency clock that increases power [2]. Current-ratio-based MEPT relies on specialized CMOS technology for body-bias tuning [3]. A switched-capacitor-based MEPT can achieve energy minimization at a targeted performance [4], but it uses a 30MHz clock with μW power consumption and low power efficiency. For ULP IoT applications, SoCs need to have ultra-low quiescent power, high efficiency for energy delivery, performance scaling based on available energy, and energy minimization to increase system lifetime. In this work, we propose an ULP IoT SoC with a triple-mode power management unit (PMU) that integrates energy-performance scaling, event-driven fast DVFS, and MEPT features to improve the system energy efficiency, as shown in Fig.13.8.1. This work achieves a minimum 194nW power consumption for the SoC and 5.2nW quiescent power for the PMU with a 92.6% peak efficiency and $>10^4$ dynamic range. The timing waveform in Fig.13.8.1 (bottom), demonstrates the transition of the three modes including energy aware (EA), performance aware (PA), and MEPT based on event priority and input voltage level which reflects the energy availability. As such, the system energy consumption and performance could be well-balanced based on both the input and output conditions.

Figure 13.8.2 shows the architecture of the SoC, which comprises a microprocessor (MCU) with a 32b RISC-V core, a boot ROM, peripherals, a memory controller, and an 8KB SRAM, along with a clock and reset generation block, a buck converter with hybrid control scheme [5], a voltage monitor (VM), a MEPT block, and a mode control (MC) block. For performance awareness, the MCU keeps monitoring the I/O interfaces and mapping the event priority to the last 4 bits of SEL_{PA} signal (SEL_{PA4}). The most significant bit (MSB) of SEL_{PA} is the comparison result of SEL_{EA} and SEL_{PA4}. For EA mode, the VM is clocked by a leakage based current starving OSC (CS-OSC) to continuously monitor the input voltage through a 4b asynchronous SAR ADC. To reduce the power to sub-nW while sampling the voltage value from 1.5 to 2.5V within a 62.5mV ADC resolution, the V_{IN} is divided by 3 and then compared with two voltage references, V_H and V_L. In MEPT mode, the MEPT block tracks the MEP and controls the V_{REF} through SEL_M. The buck control circuits adopted from [5] utilize a hybrid async./sync. control scheme to enable fast DVFS tracking and fast load transient response (FLTR) with pW-level power. The Buck Converter block includes two pulse generators and a power stage with tunable length for efficient power delivery. To achieve low quiescent power, the entire PMU uses a customized 2.5V I/O device standard-cell library except for the MEPT block that uses high V_{TH} CMOS. The proposed triple mode control algorithm is shown in Fig.13.8.2 (bottom-left). By default, the system is in EA mode where SEL equals SEL_{EA} and the V_{OUT} is adjusted based on energy availability. When SEL_{PA4} becomes larger than SEL, which indicates a need for higher performance, the EN_{DVFS} and MSB of SEL_{PA} go up to 1 to quickly push the PMU into PA mode. Then the V_{OUT} gets tied to the event priority to regulate performance. Similarly, if the $SEL_{PA4}<SEL_{EA}$ in PA mode, the system goes back to EA mode for energy saving. When SEL_{EA} is lower than a threshold, which indicates the system is running out of energy, the PMU goes into MEPT mode and SEL equals to SEL_M. Therefore, by monitoring the input and output condition using SEL_{EA} and SEL_{PA} signals, the PMU can achieve power-performance scaling. The proposed CEC MEPT algorithm is shown in Fig.13.8.2 (bottom-right). Entering the MEPT mode, the V_{REF} is set at the highest value, 580mV. After 16 cycles of EN_{BUCK}, the $counter_H$ and $counter_L$ are enabled to count the digital clock cycles during one EN_{BUCK} cycle at adjacent two V_{OUT} values, respectively. Finally, the two counters are compared to decide the direction of the MEPT.

Figure 13.8.3 shows circuit implementation and principles of CEC MEPT. The MEPT reuses the existing PMU circuits and only needs two 11b asynchronous counters, a MEPT algorithm block, a pulse generator and 3b level shifters. To achieve MEPT with high tracking accuracy, low power and minimal area, several techniques are used: 1) the proposed CEC MEPT algorithm reuses the two existing EN_{BUCK} and CLK_{DIG} signals to track the MEP without any extra clocks or voltages; 2) The full digital implementation with EN_{BUCK} as a slow clock signal for synchronous algorithm block and CLK_{DIG} as a fast clock signal for asynchronous counters, enables the MEPT block to fully function for V_{OUT} down to 0.4V, which significantly saves power; 3) The CLK_{BUCK} is regulated at a fixed higher frequency to minimize the MEPT errors caused by V_{OUT} ripple variations. The timing waveform shows the proposed MEPT principles. The energy per cycle (E_{PC}) can be calculated using the equation in Fig.13.8.3 (top-right) where the constant energy delivered to the load is divided by the number of cycles the load runs, M_{count}. The constant values include the inductance value L, the timing length of the power stage on-time T_{HS} and the cycle of EN_{BUCK} N, which is 1 in this design. Although the V_{OUT} and power efficiency η_{effi} are variables, the errors caused by them are negligible. The difference between two consecutive V_{OUT} transition is small such that the largest error caused by the V_{OUT} is as low as 2.2%, when V_{IN} is 1.5V and V_{OUT} changes from 0.58 to 0.56V. Furthermore, the buck converter efficiency decreases when V_{OUT} gets smaller which further reduces the E_{PC} error below 2.2%. Measurement results in Fig.13.8.3 (bottom-left), demonstrate the effectiveness of the proposed MEPT against load variation. The MEPT result is the mode value of MEPT results over 20 iterations. The proposed circuits can find the real MEP within 20mV for varying dynamic loads, allowing operation very close to the true minimum E_{PC}. With all these techniques, the MEPT block achieves 379pW idle power and 412pW active power at $0.5V_{OUT}$ with a 0.026mm² area overhead.

This SoC is fabricated in a bulk planar 65nm CMOS process. Figure13.8.4 shows the triple mode transition waveform. When V_{IN} increases, the PMU leaves MEPT mode and enters EA mode. Since the SEL_{EA} is still relatively small, the PMU goes into PA mode whenever an event occurs. When V_{IN} increases above 2V, the low priority events cannot trigger the PA mode, since SEL_{EA} is larger than the mapped SEL_{PA4} indicating the performance requirements are satisfied. After the V_{IN} goes to 1.5V, the MEPT block starts tracking to keep the system operating at the MEP until V_{IN} charges up again or an event occurs.

Figure 13.8.5 shows the measured PMU efficiency across V_{IN} and V_{OUT} using the equation P_{OUT}/P_{PMU} where the MEPT is powered by V_{OUT}. The PMU achieves 92.6% peak efficiency and maintains an efficiency >80% from 190nW to 3mW providing over 10^4 of load power range. The top-right of Fig.13.8.5 shows the MEPT accuracy across dies. 10 chips are tested with the pseudo loads and tunable-replica OSC as loading components and the results show that the maximal voltage error is <18mV and the maximal E_{PC} error is <2.3%. The bottom of Fig.13.8.5 shows the system and PMU power breakdown. The SoC has a minimum system power consumption of 194.3nW at 180Hz clocked by a CS-OSC and the proposed PMU achieves 5.2nW quiescent power. The MEPT circuits power overhead in the idle state only account for 0.19% of the total system power.

Figure 13.8.6 compares our work to state-of-the-art works, which have not previously targeted the nanowatt level power range. Our PMU maintains a high efficiency over a load range that is >100× than the prior art and achieves the highest peak efficiency. Thanks to the hybrid buck control scheme, this PMU also features fast DVFS and FLTR which previous works do not support. The CEC MEPT circuit achieves <2.3% E_{PC} error with >100× power overhead reduction and the lowest area. Finally, the SoC and PMU achieve MEPT for energy minimization, performance regulation, and available input energy awareness while simultaneously allowing these techniques to be applied to ULP, nW-scale SoCs. All these results and features make this SoC well-suited for ULP IoT applications. Figure13.8.7 shows a micrograph of the SoC with a 1.56×2.19mm² die area.

Acknowledgments:
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[4] J. Lee, et al., "A 6.4pJ/Cycle Self-Tuning Cortex-M0 IoT Processor Based on Leakage-Ratio Measurement for Energy-Optimal Operation Across Wide-Range PVT Variation," *ISSCC Dig. Tech. Papers*, pp. 314-315, Feb. 2019.
[5] Xinjian Liu, et al., "An 802pW 93% Peak Efficiency Buck Converter with 5.5×106 Dynamic Range Featuring Fast DVFS and Asynchronous Load-Transient Control," *IEEE ESSCIRC,* pp. 347-350, 2021.

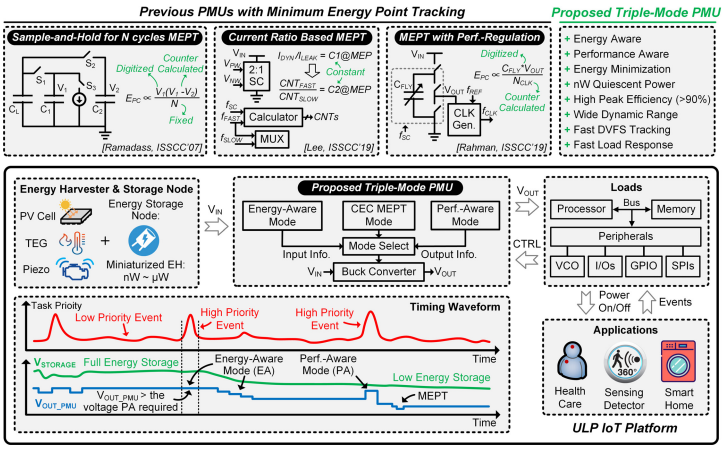

Figure 13.8.1: Comparison of the prior-art PMUs integrated with MEPT (top); an ultra-low power IoT platform with the proposed triple-mode power management for energy-efficient operations demonstrating mode-transition scenarios (bottom).

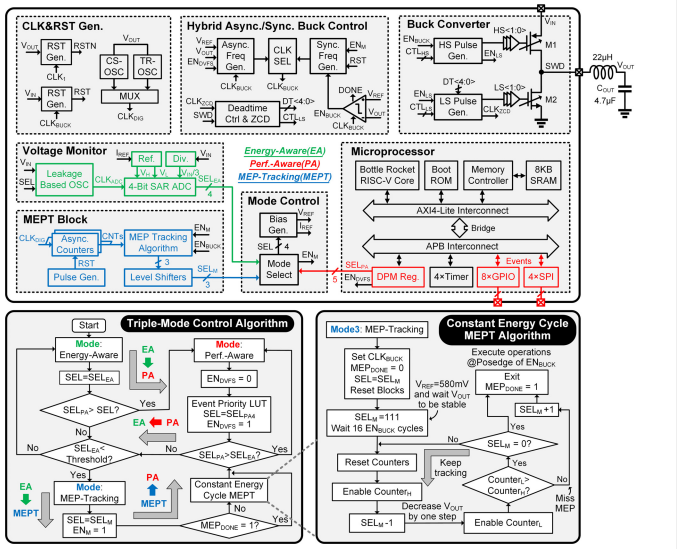

Figure 13.8.2: System block diagram of the ULP IoT SoC with the proposed triple-mode PMU (top); flow chart of the proposed triple-mode control algorithm (bottom-left); flow chart of the proposed CEC MEPT algorithm (bottom-right).

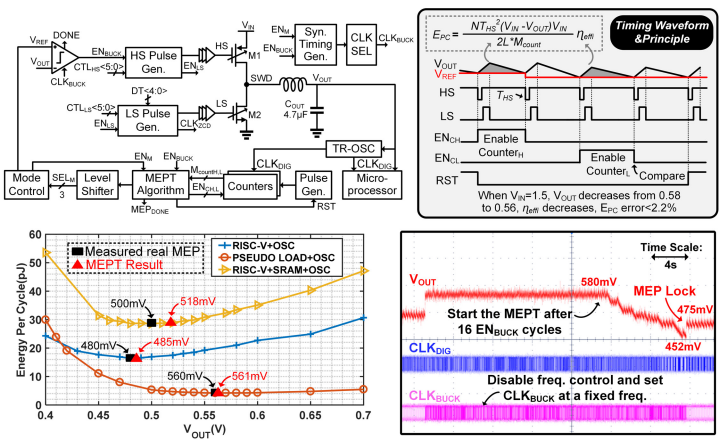

Figure 13.8.3: Schematic of the buck converter with MEPT and operation timing diagram of the proposed CEC MEPT (top); measured MEP tracking accuracy across different loading components and measured MEPT timing waveform (bottom).

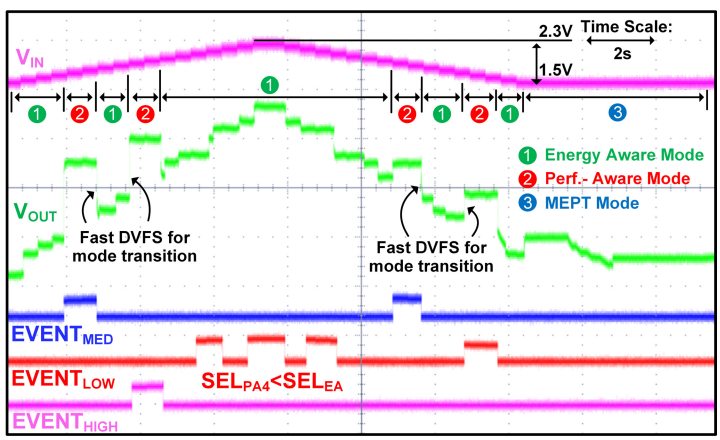

Figure 13.8.4: Measured triple-mode transitions demonstrating energy-awareness with V_{IN} changes between 1.5V and 2.3V, performance-awareness with three prioritized input events, and MEPT when V_{IN} is reduced to 1.5V.

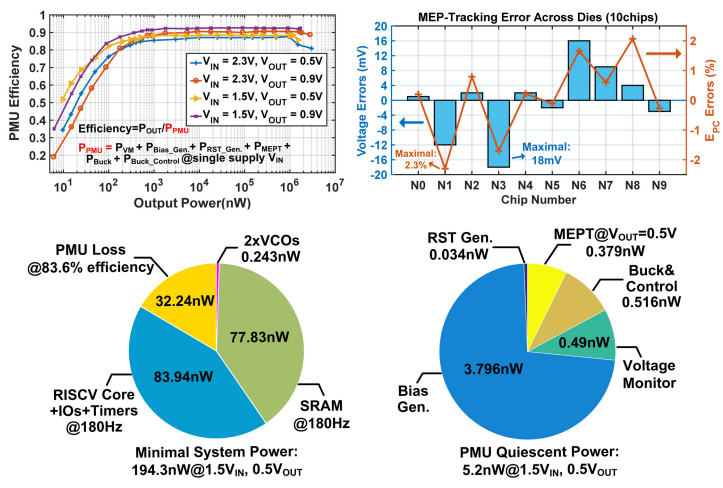

Figure 13.8.5: Measured PMU efficiency versus P_{OUT} across different V_{IN} and V_{OUT} and measured MEPT voltage and energy per cycle errors across 10 chips (top); measured SoC system power breakdown at 180Hz and measured PMU quiescent power breakdown at V_{IN} = 1.5V and V_{OUT} = 0.5V (bottom).

	[2] ISSCC'07	[3] ISSCC'19	[4] ISSCC'19	This Work
Technology	65nm	55nm CCD	65nm	**65nm**
Processor and SRAM	N/A	Cortex-M0+8KB	Cortex-M3+512B	**RISC-V+8KB**
Regulated Voltage (V)	0.25-0.7	0.48-0.75	0.35-0.58	**0.4-1.1**
Operating Frequency	N/R	100KHz-6MHz	1.1Hz-38MHz	**180Hz-5.7MHz**
PMU Architecture	Sync. Buck	Cascade SC	C_{FLY} Tuned SC	**Async./Sync. Buck**
Power Management Techniques	MEPT	MEPT	MEPT+Perf. Aware	**MEPT+Perf. Aware +Energy Aware**
MEPT voltage error/E_{PC} error	N/R	<4.7%	≤5mV	**<20mV/<2.3%**
MEPT Power Consumption	N/R	84nW*	2μW	**412pW**
MEPT Area	0.05mm^2	N/R	0.043mm^2	**0.026mm^2**
Fast DVFS	No	No	No	**Yes**
Fast load Response	No	No	No	**Yes**
Dynamic Load Range with Efficiency > 80%	1μW-100μW (100)	N/R	N/R	**190nW-3mW (1.57x10^4)**
PMU Peak Efficiency (%)	86	N/R	82*	**92.6**
System Power Consumption	1.23μW-116.2μW*	>110nW*	>2.4μW*	**194.3nW-598.6μW**
Components included in Minimal System Power	PMU+FIR	Cortex-M0+SRAM +CLK+TIMER	N/R	**RISCV+SRAM+IOs+ PMU+TIMERs+ROM+CLK**

*Calculated/Observed from waveforms

Figure 13.8.6: Comparison of the proposed PMU-enabled IoT SoC with prior art.

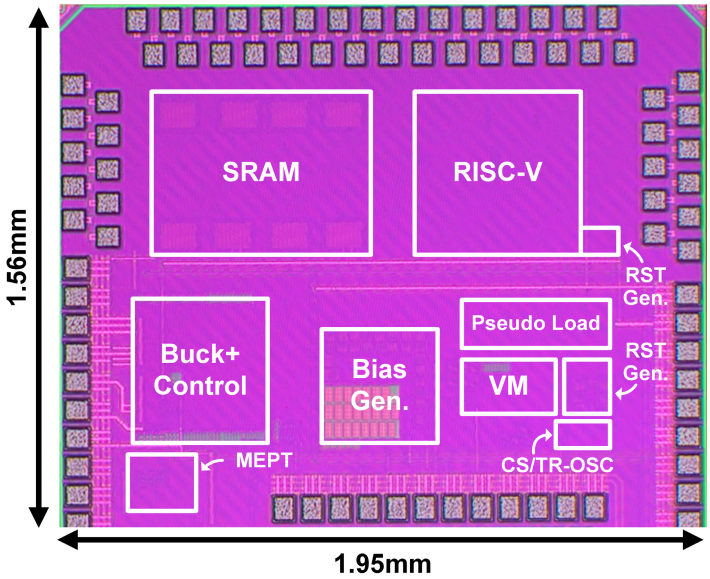

Figure 13.8.7: Die photo of the ULP IoT SoC.

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