A 33nW Fully Autonomous SoC with Distributed Cooperative Energy Harvesting and Multi-Chip Power Management for mm-scale System-in-Fiber

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***Abstract*— This paper presents a fully autonomous system-on-chip (SoC) that can be distributed along a fiber strand, capable of simultaneously harvesting energy, cooperatively scaling performance, sharing power, and booting-up with other in-fiber SoCs for ultra-low-power (ULP) sensing applications. Utilizing a custom switched capacitor energy harvesting and power management unit (EHPMU), the SoC can efficiently redistribute and reuse harvested energy along the fiber. Integrated on-chip, the ULP RISC-V digital core and temperature sensor enable energy-efficient sensing and computation at nanowatt power levels. A dedicated ripple boot-up and cooperative dynamic voltage and frequency scaling (DVFS) further optimize the operation and physical size of the system. Fabricated in 65 nm, measurement results show that the proposed SoC achieves 33 nW power consumption for the whole chip under 92 Lux lighting condition and can reduce control power down to 2.7 nW for the EHPMU. With the proposed power sharing and cooperative DVFS techniques, the SoC reduces the illuminance needed to stay alive by >7× down to 12 Lux. Integrated into a mm-scale polymer fiber, our SoC demonstrates the feasibility of fully autonomous and ULP on-body sensing systems in resource-constrained fiber environments.**

***Index Terms*—Self-powered system-on-chip, distributed sensing network, power management, energy harvesting, power sharing, ultra-low-power, ripple boot-up, DVFS.**

I. INTRODUCTION

The increasing popularity of mobile digital computing systems, known as wearables, has paved the way for collecting physiological data from the human body. However, these wearable devices often require users to carry an additional rigid object, limiting their adoption and restricting the data they can access. In contrast, everyday clothing provides a distinct advantage as it maintains a direct contact with larger areas of the body. This presents a significant opportunity to collect, store, and analyze untapped physiological variables. With the rapid advancements in integrated circuit (IC) technology, especially reductions in power consumption and physical size, miniaturized self-powered systems can be seamlessly integrated into textiles or a single fiber strand [1]-[6]. These miniaturized self-powered systems-in-fiber (SiFs) offer significant potential for enabling various new sensing applications, such as health monitoring, human-computer interfaces, and on-body machine-learning. This trend enables continuous in-fiber background monitoring of physiological and environmental signals without the need for external power sources, constraints related to space limitations, frequent battery replacements, or regular maintenance.

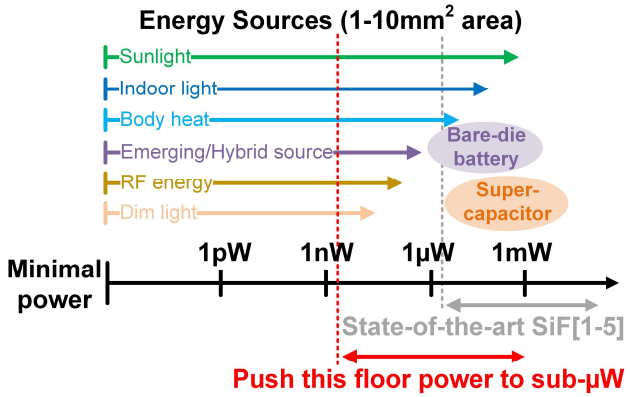

Fig. 1. The available energy from different types of energy sources in a 1-10 mm^2 scale form factor, including thermal energy [8], solar energy [9][10], RF energy [11], other emerging and hybrid energy sources [12], coin batteries [13], and supercapacitors [13].

However, to build such a self-powered, imperceptible, lightweight, and robust SiF in a mm-scale form factor, the design of the systems-on-chip (SoCs) presents significant challenges: 1) Ultra-low-power (ULP): the limited physical size of the devices severely restricts the available energy budget. As shown in Fig. 1, the available energy from various harvesting sources can vary due to environmental changes and body movements with the potential to drop to nanowatt (nW) levels. Miniaturized batteries and supercapacitors [13] only provide mAh capacity which can be depleted frequently and recharged slowly by these mm-scale harvesters, limiting the system availability. This necessitates aggressive power

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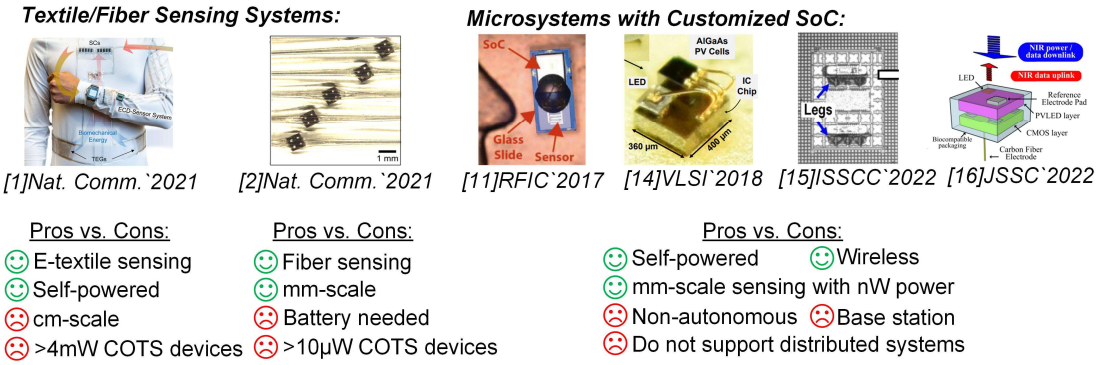

Fig. 2. The state-of-the-art textile/fiber-based sensing systems [1][2] and microsystems with customized SoC [11][14]-[16].

reduction of the SoC to match the available input energy. 2) Miniaturization: the total device count and off-chip components must be reduced and miniaturized to fit the mm-scale form factor, ensuring imperceptible and comfortable user experiences. This requires high-level integration and avoidance of bulky components, such as inductors [17]. 3) Adaptability and autonomy: the limited energy storage and versatile environment result in unreliable and intermittent harvested energy. Consequently, SoCs require adaptability and autonomy to adjust their power and performance dynamically, enhancing system reliability to avoid system shutdown. 4) Efficient sensing, computation, and communication: with a limited energy budget, it is crucial to sense, process, and transfer the collected dataset in an energy efficient manner while meeting the application demands.

Fig. 2 shows several previous works in SoC design and textile sensing systems. Each work offers some unique benefits, but none can fully deliver the performance required to enable fully autonomous mm-scale SiF. A prior smart E-textile system [1] enables self-powered on-body Na^+ sensing with energy harvested from sweat-based bioenergy, body heat, and body movement. But the system is built with cm-scale commercial-off-the-shelf (COTS) components that consume >4 mW. The work presented in [2] achieves mm-scale in-fiber body temperature sensing and data storage, enabling healthcare monitoring and human activity recognition using embedded temperature sensors and memories. However, this intelligent fiber requires batteries as energy sources with >10 μW power consumption. The state-of-the-art microsystems that use custom SoCs have achieved nW power and mm-scale form factor [11][14]-[16]. They enable ULP glucose concentration sensing [11], temperature sensing [14][15], and neural recording [16]. However, these microsystems all need a dedicated base station to provide light (>3 Klux [14], >60 Klux [14]) to program, communicate, and power the devices wirelessly. Moreover, none of them support communication in a distributed system. This leads to reduced system autonomy and an inability for direct inter-SoC communication. Therefore, to address these limitations, we propose a fully autonomous self-powered SoC that can be distributed along a fiber strand, capable of simultaneously harvesting energy, cooperatively scaling performance, sharing power, communicating, and booting-up with other SoCs to enable a self-supporting networked sensing system in-fiber, as shown in Fig. 3.

The highlighted advantages and innovations beyond the prior art include:

1. Distributed harvesting: instead of powering the system from an aggregated energy source, the proposed architecture distributes SoCs along the fiber, which enables each SoC to harvest and manage energy simultaneously in a cooperative manner.
2. Power sharing (PS): All the SoCs share a supply voltage rail, the V_{SHARE} rail. Each SoC can charge, utilize, or isolate the V_{SHARE} rail. This capability provides a flexible set of power management options to redistribute and reuse the energy harvested along the fiber.
3. Ripple boot-up (RB) procedure: instead of programming each SoC individually [11][14]-[16][23], a power-gateable ripple boot-up RAM (RB-RAM) enables autonomous instruction memory programming via a RB procedure from a single non-volatile memory (NVM), achieving a minimal device count and asynchronous communication.
4. Cooperative dynamic voltage and frequency scaling (DVFS): The SoCs can monitor the energy conditions of neighboring SoCs and adjust their DVFS operating points cooperatively, which improves the viability of the entire system.
5. ULP digital core and sensor: the SoC incorporates a state-of-the-art digital core [18] based on dynamic-leakage-suppression (DLS) technology and a pW-level temperature sensor [29]. These ULP components ensure energy-efficient operation of the SoCs, significantly reducing the floor power.

With all these functions integrated on-chip, the SoC achieves 33 nW power consumption for the whole chip under 92 Lux light from a mm-scale solar cell and can reduce control power down to 2.7 nW for the energy harvesting and power management unit (EHPMU). The proposed PS and cooperative DVFS reduce the illuminance needed to stay alive by over 7× down to 12 Lux for a multi-SoC SiF versus just a standalone SoC. This allows the SoC to survive in worse lighting conditions than the prior art. We integrate the SoC into a 2.2×1 mm cross-section polymer fiber with an embedded electrical bus via a 4.7×3.7 mm interposer board, showing its compatibility with advanced fiber fabrication processes, as shown in the bottom of Fig. 3. In this paper, we expand our previous work [19] to further illustrate the design

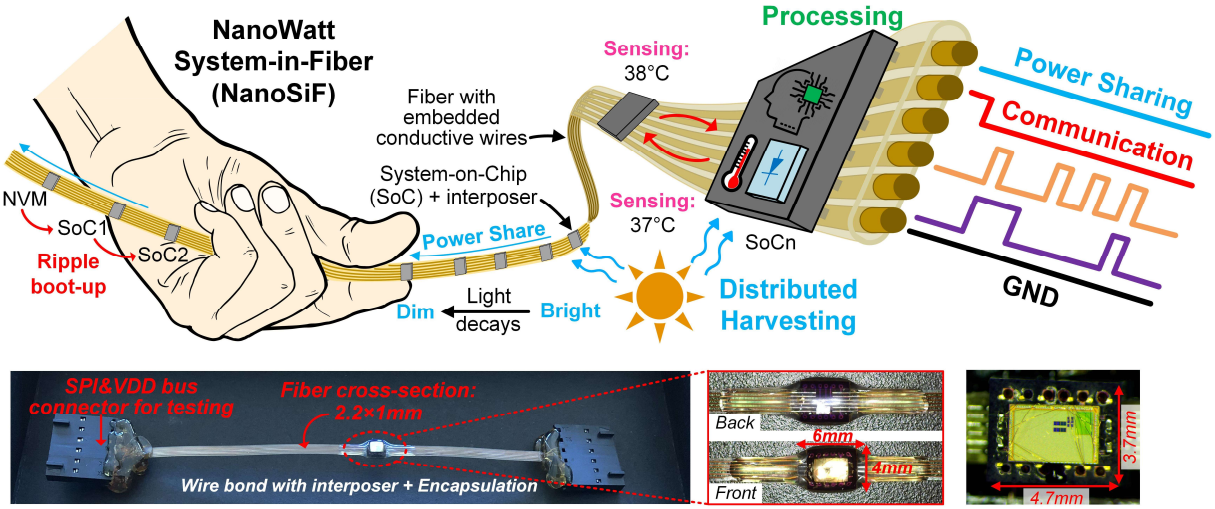

Fig. 3. Architecture of the proposed nanowatt System-in-Fiber (nanoSiF) and photos of SoC integration into a fiber using an interposer.

details, trade-offs, and circuit implementations. The subsequent sections are organized as follows: Section II presents an overview of the system architecture, system-level behaviors and background of the technologies that are used. Section III demonstrates the detailed circuit implementation, followed by the silicon measurements and fiber integration in Section IV. Finally, Section V concludes this paper.

II. System Behavior and Technology Background

A. Architecture of the Proposed System and SoC

Fig. 3 and Fig. 4 show the connectivity and architecture of the proposed nanowatt system-in-fiber (nanoSiF). To enable self-powered sensing, processing, and communicating, each SoC is composed of a digital core, EHPMU, temperature sensor, RB-RAM, and other supporting blocks. Fig. 4 shows how all the SoCs share a voltage rail, the V_{SHARE} rail, while each SoC also has its own dedicated local rails, to power the components on the local chip. This design allows for a highly flexible set of power management options. Further details on this power management are presented in Section II-B. In addition to the shared V_{SHARE} and ground rail, the SoCs are interconnected to upstream and downstream SoCs via serial peripheral interfaces (SPI). This connection setup requires only six signals, including V_{SHARE}, SPI signals (SS, SCLK, MOSI, MISO), and GND. With the proposed RB-RAM, as described in Section II-C, a compact in-fiber communication solution can be realized for applications with limited space availability.

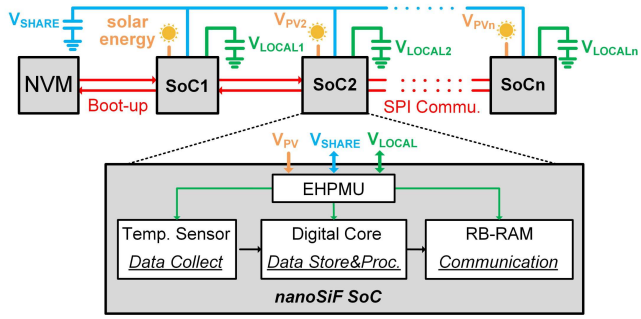

Fig. 4. The connectivity of the SoCs and architecture of the proposed nanoSiF.

B. Distributed Harvesting and Power Sharing

Instead of powering the entire fiber system from a centralized energy source, the proposed nanoSiF adopts a distributed energy harvesting and PS approach. This approach involves strategically placing the SoCs along the fiber strand to enable cooperative and simultaneous energy harvesting. Each SoC can dynamically adjust its connectivity among the EHPMU, V_{SHARE}, and V_{LOCAL} rails. The EHPMU works in three different modes, as shown in Fig. 5(a). For mode 1, the V_{SHARE} and V_{LOCAL} rails are shorted together, allowing the EHPMU to interact with both rails simultaneously. In mode 2 and 3, the EHPMU only interacts with one rail (the V_{SHARE} or V_{LOCAL} rail), respectively, while the two rails remain disconnected.

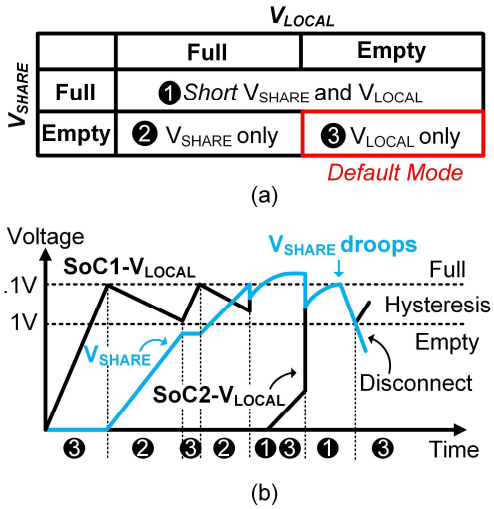

Fig. 5. The principle of the power sharing control scheme: (a) three different modes; (b) timing waveform for mode transition.

These functions enable a flexible set of power management options. With an integrated step-up/down converter, SoCs can charge surplus energy to the V_{SHARE} rail when it is available, draw power from the V_{SHARE} rail when local energy is scarce, or isolate the chip from the V_{SHARE} rail to act as a power island. Fig. 5(b) shows the timing waveform of the proposed PS scheme. By default, mode 3 is activated, and the EHPMU

only charges the V_{LOCAL} rail to power the components on the local chip. Once the V_{LOCAL} rail reaches 1.1 V, indicating the local storage node is full, the SoC switches to mode 2 to contribute the surplus energy to the V_{SHARE} rail. During this transition, the V_{LOCAL} rail keeps powering components on the local chip without being charged, causing it to gradually drop below 1 V. Then, the SoC re-enters mode 2 to regulate the V_{LOCAL} rail, guaranteeing the functionality of the SoC itself. Once both rails are full, the SoC connects them together for reduced voltage rippling. Notably, an additional benefit of this PS scheme is its ability to accelerate the cold startup time when the V_{SHARE} rail is already fully charged. As shown in Fig. 5, the SoC2 achieves a faster startup operation. Moreover, in situations where other SoCs are drawing excessive power from the V_{SHARE} rail, causing the V_{SHARE} rail collapsing, the two SoCs isolate their V_{LOCAL} rails from the V_{SHARE} rail to act as independent power islands. In this way, local regions of the fiber can stay active even when other regions are experiencing power shortages. Compared to the centralized architecture, although this distributed architecture introduces cascade loss during power sharing due to the energy transfer into the V_{SHARE} rail and subsequent down-conversion, yet it reduces the system's reliance on a single centralized PV cell. This improved system viability ensures uninterrupted functionality. Additionally, the distributed architecture provides greater flexibility in power management, ensuring surplus energy from SoCs with higher light intensity benefits those in dimmer environments. Consequently, the overall energy efficiency and energy utilization of the self-powered SiF are optimized.

C. Ripple Boot-up and Asynchronous Communication

In addition to the energy challenges, efficient in-fiber communication and SoC programming present another barrier. Conventionally, each SoC requires to be programmed individually [11][14]-[16] or paired with a dedicated non-volatile memory (NVM) [23], which is impractical for SiF applications due to the physical size constraints.

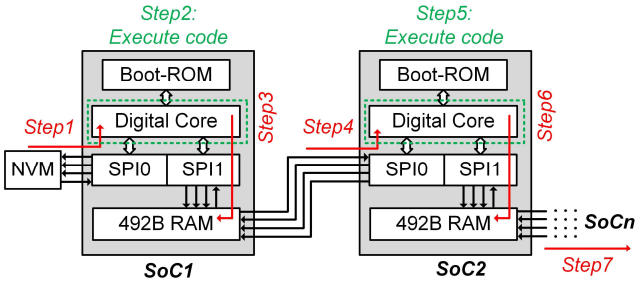

Fig. 6. Ripple boot-up procedure and principle.

To address this limitation, we propose an RB procedure to program all the SoCs in-fiber, using only one NVM. Fig. 6 illustrates the RB procedure. Each SoC incorporates two SPI masters (SPI0 and SPI1) and a 492-byte RB-RAM. In the RB procedure, after the first SoC in the fiber starts up, it executes its boot-ROM code which uses SPI0 to load the intended program from the adjacent NVM into its own instruction memory for execution. It additionally copies the newly loaded instruction code into its RB-RAM over SPI1, as illustrated by steps 1-3. The original instruction code may be programmed to follow an evolution during this propagation, such as incrementing a register value to be used as a unique chip identifier. In other words, SoC1 can put either the same or a modified version of its own instruction code into its RB-RAM. When the second SoC (SoC2) starts up, it loads the program from the RB-RAM of SoC1 and copies the program into its own RB-RAM, ensuring the downstream SoC (SoC3) can load the program. This process is repeated, enabling all the SoCs in the fiber to receive their program using only one NVM, which reduces the device count. Furthermore, the RB-RAM facilitates inter-SoC asynchronous communication. Each SoC can read and modify the RB-RAM of the upstream SoC and its local RB-RAM, ensuring that the neighboring SoCs are aware of the updated information. In our implementation, the RB-RAMs are small for supporting simple operations, but this scheme can scale up to larger instruction memories.

D. Cooperative DVFS

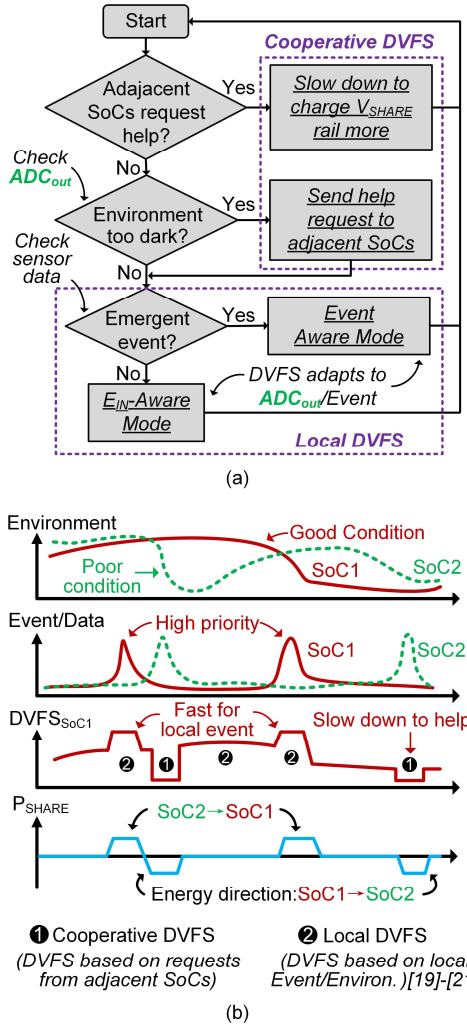

Fig. 7. (a) the proposed cooperative and local DVFS control algorithms; (b) the timing waveform of the proposed cooperative and local DVFS control.

Conventionally, DVFS is used to balance the power consumption and performance of the SoC [20]-[22]. Frequency and voltage can be dynamically scaled according to either the input energy condition, task priority, or a combination of both. With the proposed RB-RAM and PS technology, the SoC can share energy and data with other in-fiber SoCs. These advantages enable the SoCs to cooperatively scale their power and performance not only

based on the local energy/task conditions but also considering the conditions of adjacent SoCs. This cooperative DVFS approach facilitates global performance and energy optimization, maximizing the overall viability of the system.

Fig. 7 (a) shows the proposed cooperative and local DVFS control algorithms. Each SoC periodically updates a register in its RB-RAM that indicates whether its local environment is too poor and in need of an energy boost. Adjacent SoCs periodically detect whether there is a help request from neighboring SoCs and assess their local energy conditions. If a help request is detected, the SoC moves into cooperative DVFS mode and slows its clock frequency down to reduce power and share more energy with the V_{SHARE} rail. Conversely, if its local environment is poor, the SoC updates its RB-RAM to indicate a help request and then moves to local DVFS mode to reduce its clock speed and power consumption, conserving energy. Therefore, by adopting this approach, when certain SoCs face critical harvesting conditions, adjacent SoCs can slow down their operations to share more power, ensuring the entire fiber system remains operational. Fig. 7 (b) shows the proposed cooperative and local DVFS control timing waveforms. The four rows represent the environment condition, event priority (data amount), DVFS operating speed of SoC1, and energy flow direction, respectively. When the environment is in a good condition and there are no help requests from adjacent SoCs, SoC1 scales its performance and power according to the environment or event priority, operating in local DVFS mode. However, if its local environment falls below a critical threshold or the adjacent SoCs request help, SoC1 moves into cooperative DVFS mode.

E. Dynamic Leakage Suppression Technology

To maintain continuous battery-less sensing, the SoC needs to dynamically scale its performance in response to the fluctuating input energy conditions, even down to the low-nW level. However, the floor power of a static CMOS logic based MCU/SoC is limited to 100 s of nW range due to leakage power, unless it has a dedicated retention mode [24] or deep-sleep mode [25]. DLS logic [26] can push the floor power down to a few nW, but it suffers from poor performance scaling due to a weak dependence on the supply voltage. As shown in Fig. 8, scalable DLS (SDLS) logics are then introduced to transition each gate across a continuous range between DLS and CMOS operating regimes [18][27] over the two bias voltage, V_{CN} and V_{CP}. This provides granular performance scalability while still maintaining the floor power of the SoC at a few nW.

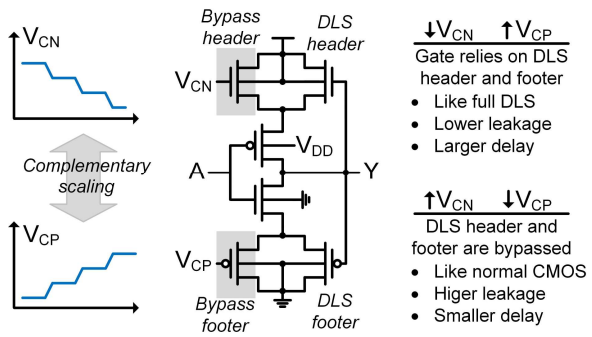

Fig. 8. Scalable DLS logic architecture and working principle [18][27].

In this design, the processor is synthesized with a customized SDLS standard cell library for ULP and scalability. In addition, memory is a crucial component for storing data and instructions, but conventional SRAM has high leakage current and nW-level memory either suffers from low density due to the latch-based cells [14] or requires a dedicated deeply depleted process [20]. In this design, DLS logic is utilized in the SRAM bit cell to achieve nW-level power consumption and improved noise margin [28]. Furthermore, positive overdrive voltage ($V_{SG}< 0$) is used for the access transistor in the bit cell, reducing leakage current by 332-3117× from 0.3-0.9 V compared with the conventional 6T bit cell [28].

In total, the combination of flexible power management options, asynchronous communication through the RB-RAM, cooperative DVFS, and (S)DLS technologies enables the SoCs to achieve efficient power utilization, compact in-fiber communication, optimized energy-performance balance, and ULP floor power.

III. Circuit Implementation

A. System Implementation

Fig. 9 shows the block diagram of the proposed nanoSiF SoC. It is composed of a digital core (described in our previous work [18]), a two-stage switched capacitor (SC)-based EHPMU, a sub-nW temperature sensor [29], a DVFS controller, I/O peripherals, and an RB-RAM. The EHPMU harvests energy from a photovoltaic cell (PV) through a two-stage SC-based converter and low-dropout regulator (LDO) to generate four outputs: V_{DIG} (~0.58V), V_{LOCAL} (1-1.2V), V_{SHARE} (1-1.2V), and V_{LDO} (0.95V). The cold startup function and two-dimensional maximal power point tracking (2D-MPPT) are integrated into the EHPMU to achieve full autonomy and adaptability. The peripherals in the digital core include two SPI masters, an 8-bit GPIO port, and 7 memory-mapped registers (32-bit). These components facilitate wireline communication between SoCs and enable observation and communication with the on-chip components. SPI0 is connected to the upstream SoC, and SPI1 is connected to its local RB-RAM for asynchronous communication and ripple boot-up. The temperature sensor utilizes gate leakage to achieve sub-nW power consumption with a resolution of 0.25 C [29]. The DVFS controller generates two bias voltages, V_{CN} and V_{CP}, to adjust the performance and power of the SDLS gates in the digital core. In addition, it replicates the critical path of the digital core and keeps the digital core operating at the maximum frequency. The RB-RAM incorporates two SPI slaves and a 492-byte RB-RAM to allow the local SoC and adjacent SoCs to read and write the information in the RAM for asynchronous communication.

B. Digital Core with DVFS Controller

The digital core [18] includes an SDLS-based 32-bit RISC-V processor and an 8 KB DLS SRAM. The processor implements a BottleRocket RISC-V core (RV32IMC, derived from [30]). Except for the SRAM, all components in the core are synthesized using a custom IO-device forward-body-bias SDLS standard cell library. The bit-cell for the SRAM is also implemented with all IO devices to minimize leakage. The high V_{TH} and thick gate oxide property of IO devices

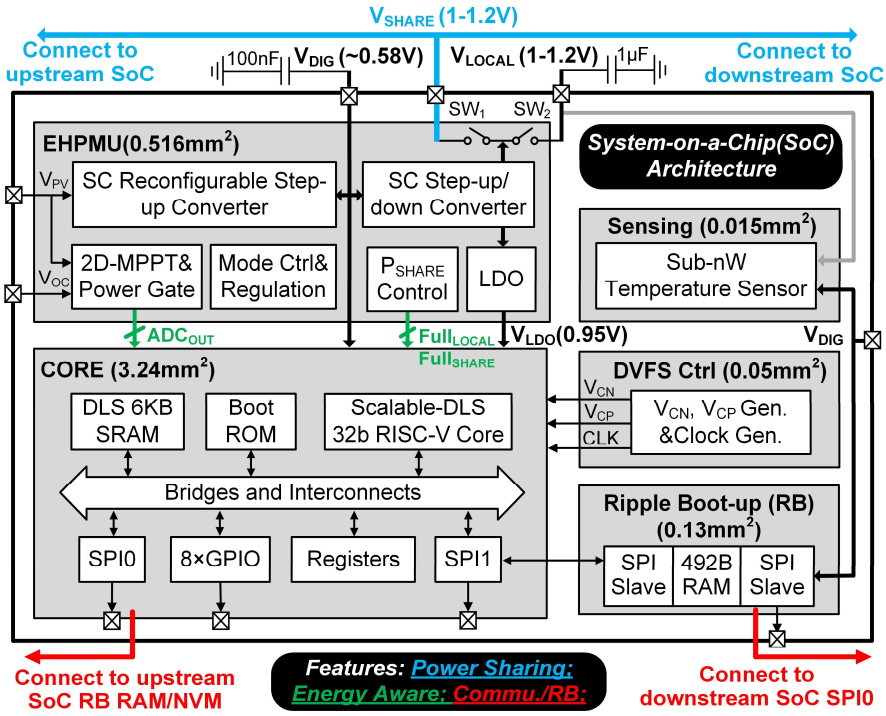

Fig. 9. The block diagram of the proposed SoC.

significantly reduce the subthreshold leakage and prevent gate leakage at high supply voltages.

The DVFS controller [18][27] consists of a voltage scaling controller (VSC) and an adaptive clock generator (ACG). The VSC generates the V_{CN} and V_{CP} voltages by selecting two complementary references from a voltage divider, followed by a pA-driver. The ACG is composed of an SDLS-based ring oscillator (OSC) bank (12 possible OSCs with different scaling characteristics to choose from), a programmable divider, and a duty cycle controller. The SDLS-based OSC tracks the max frequency of the digital core. The tunable divider and multiple OSCs provide flexibility in tuning the frequency sensitivity to V_{CN}, V_{CP}, and VDD, which helps ensure a close match between the replica path delay and the critical path of the digital core.

C. SC-based Two-stage Converter

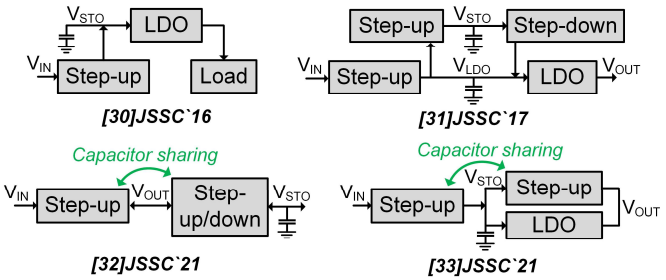

Fig. 10. The architecture of conventional SC-based multi-output EHPMUs [31]-[34].

For self-powered SiF applications, the EHPMU circuits require to be fully integrated on-chip and ULP. However, conventional inductor based EHPMU suffers from bulky off-chip inductors [17]. On the other hand, hybrid-inductor-capacitor architectures, while capable of miniaturization, typically demand power consumption in the μW-mW range. Therefore, in this design, this design leverages a SC-based EHPMU to achieve miniaturization and ultra-low quiescent power. Conventionally, four architectures are utilized for multi-output SC-based EHPMU, as shown in Fig. 10. The first approach proposed in [31] harvests energy from the PV cell and stores it in a battery and then down-converts to the V_{OUT}. However, for ULP applications where the load typically works in the near/sub-threshold region, 0.3-0.6V for example, the EHPMU has a large (>20×) cumulative ratio voltage conversion, leading to decreased end-to-end efficiency. The architecture proposed in [32] directly regulates the V_{OUT} using the harvested energy and stores the surplus energy in the battery. However, this design requires off-chip MPPT and four converters, leading to low overall efficiency and an area penalty. The recent work in [33][34] utilizes a two-stage architecture with capacitor sharing technology to avoid cascade loss and improve the flying capacitor utilization. Based on the input and output power conditions, the flying capacitors can be dynamically reallocated to the first or second stage. Nevertheless, the work in [33] does not have cold startup circuits for deployability and requires a 10 MHz clock, leading to high power overhead. Moreover, both works target μW-level which is not suitable for nanoSiF applications.

To address these limitations and enable flexible power management options, our EHPMU utilizes the two stage SC-based architecture [33] to avoid cascade loss. For the 1st stage converter, we use a reconfigurable serial-parallel charge pump with five conversion ratios, modified from [35], as shown in Fig. 11(a). This allows us to utilize a lower frequency clock with a smaller area for ULP applications, compared with the continuously scalable conversion ratio converter [33]. To accommodate the wide input voltage range, the 1st stage step-up converter supports the conversion ratios of 4×, 3×, 2.5×, 2×, and 1.5×. Moreover, devices with different threshold voltage are used to tradeoff between leakage and speed. For

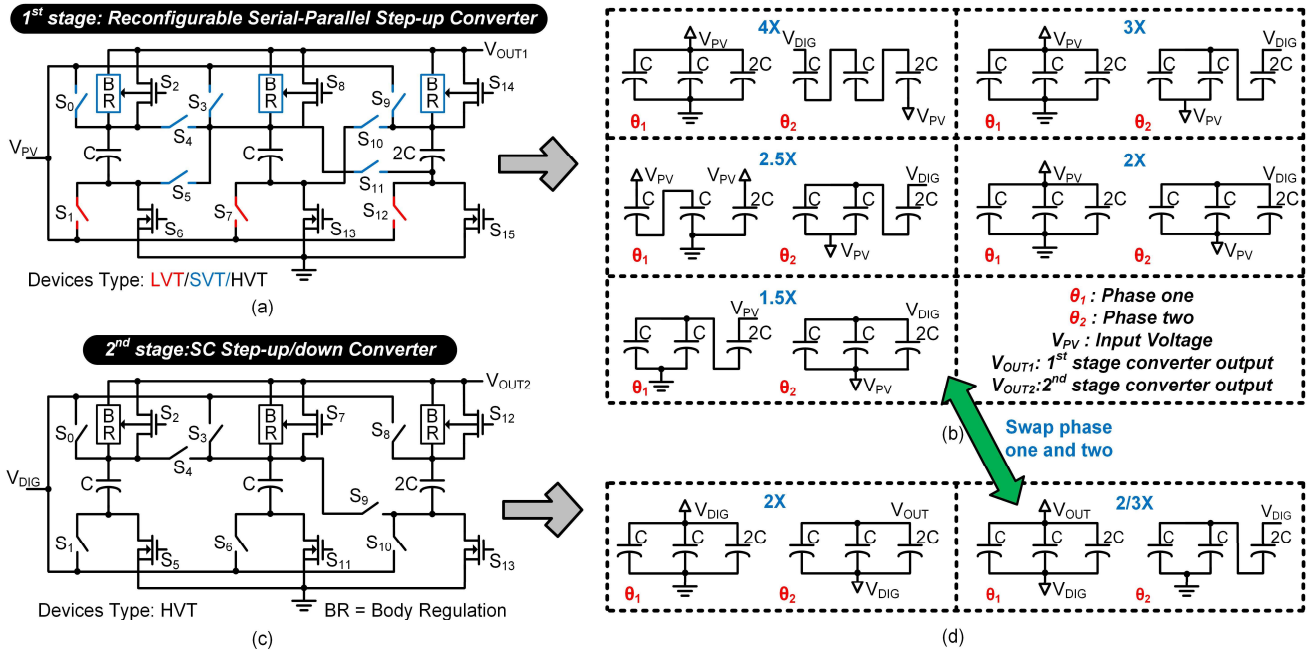

Fig. 11. (a) the schematic of the step-up converter; (b) the configurations of the step-up converter; (c) the schematic of the step-up/down converter; (d) the configurations of the step-up/down converter.

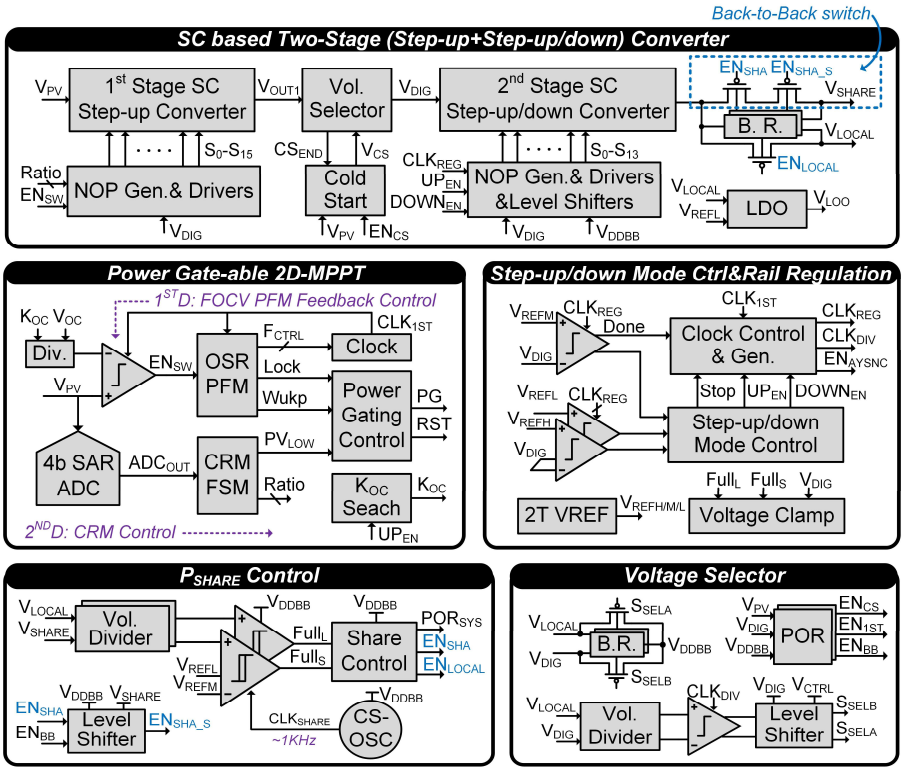

Fig. 12. The block diagram of the proposed two-stage SC EHPMU.

conventional work [35], it keeps the capacitance of the flying capacitors identical. This leads to sub-optimal utilization of the flying capacitors. In this design, as shown in Fig. 11(b), the capacitance of the flying capacitor and configurations are modified such that all three flying capacitors can be utilized in each conversion configuration, thereby improving the maximal output power. The 2nd stage step-up/down (bi-directional) converter supports a fixed 2/3× and 2× conversion ratio to interact with the V_{DIG}, V_{SHARE}, and V_{LOCAL} rails, as shown in Fig. 11(c)(d). The V_{LOCAL} rail powers a nW LDO to generate a V_{LDO} rail specifically for the DLS SRAM. With a 100 nF decoupling capacitor, the LDO achieves >42 dB power supply rejection ration across 1 KHz to 10 MHz in post-layout simulation. The 2nd stage converter can be configured to charge the surplus energy to the V_{SHARE} (V_{LOCAL}) rail or pull energy from the V_{SHARE} (V_{LOCAL}) rail to charge the V_{DIG} rail. For the 2nd stage converter, the 2× conversion ratio configuration is identical to the 1st stage converter, while the 2/3× conversion ratio has swapped phases compared to the 1st stage converter.

D. EHPMU Control Circuits

Several control circuits are employed for the two-stage converters to ensure full autonomy, self-adaptiveness, and flexible power management. The full block diagram of the EHPMU, including the control circuits, is shown in Fig. 12. Here are the details of the control circuits:

1) 2D-MPPT: The 2D-MPPT circuits include an always-on dynamic fractional open circuit voltage (FOCV) tracking scheme with pulse frequency modulation (PFM) and a conversion ratio modulation (CRM)-based control scheme, as shown in . The PFM regulates the PV cell voltage, V_{PV}, to a fraction of the open circuit voltage (i.e., $V_{PV} = K_{OC} \times V_{OC}$) [36]. It is achieved by calculating the oversample rate (OSR) and maintaining the OSR between 1.5-5× through controlling the frequency of the clock, CLK_{1ST}. The OSR is calculated based on the frequency of CLK_{1ST} and EN_{SW}. Besides, the K_{OC} is dynamically tracked by a perturb & observe (P&O) algorithm based on UP_{EN} frequency. By changing the K_{OC} and monitoring the frequency of UP_{EN}, an optimized K_{OC} can be found for maximum power extraction. To accommodate the wide range of the V_{PV}, CRM is achieved by a finite state machine (FSM) based on the output of a 4-bit analog-to-digital converter (ADC).

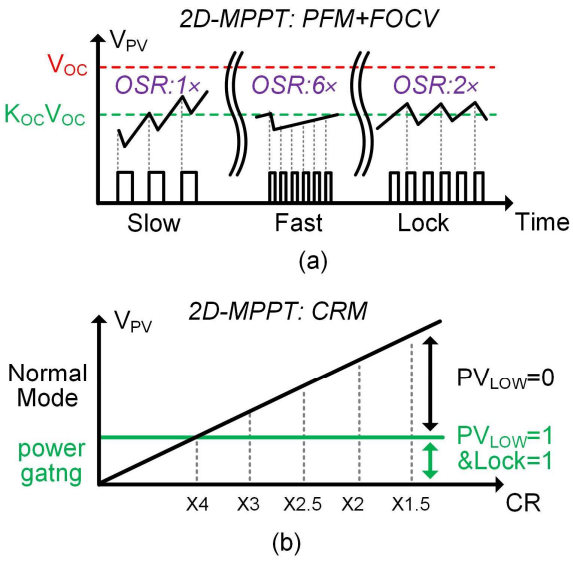

Fig. 13. The principle of the 2D-MPPT: (a) PFM+FOCV and (b) CRM.

Moreover, a power gating mode is implemented to improve the efficiency of the EHPMU in dark environments. When the V_{PV} is below a threshold, the CR is set to 4× and the PV_{LOW} signal gets activated. Once the OSR reaches a steady state for a fixed number of cycles, the signal *Lock* is activated (equal to 1). Then the 2-D MPPT goes into power-gating mode to improve efficiency in dark environments. In power gating mode, most circuits are power gated, with retention cells used to store the *Ratio* and F_{CTRL} values. The EHPMU continues to harvest energy but stops actively tracking the MPP. Once the OSR is near 0 or the maximum value, indicating the V_{PV} has drifted away from the $K_{OC} \times V_{OC}$, the *Wukp* and *RST* signal are activated to wake up and reset the circuits to retrack the MPP.

2) Step-up/down Mode Control and Rail Regulation: The EHPMU employs a step-up/down mode control and rail regulation mechanism to manage the V_{DIG} rail. It uses three digital comparators with different voltage references: V_{REFH}, V_{REFM}, and V_{REFL} for monitoring the rails. A hysteresis regulation mechanism is utilized to regulate the rail between V_{REFH} and V_{REFL}. By default, the clock of the comparator, CLK_{REG}, is divided (1/8) from the CLK_{1ST} and the 2nd stage converter is in standby mode when not actively required, for energy saving. When the V_{DIG} is above the V_{REFH} or below the V_{REFL}, the 2nd stage converter is activated, pulling the V_{DIG} rail back to the desired voltage range, as shown in Fig. 14.

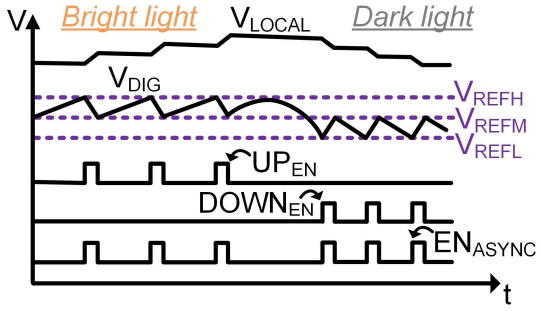

Fig. 14. The operation principle and timing waveform of the step-up/down mode control and rail regulation.

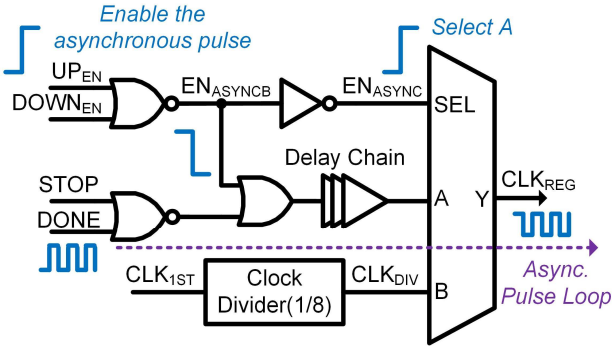

Fig. 15. The schematic of the clock control and generation for the step-up/down converter.

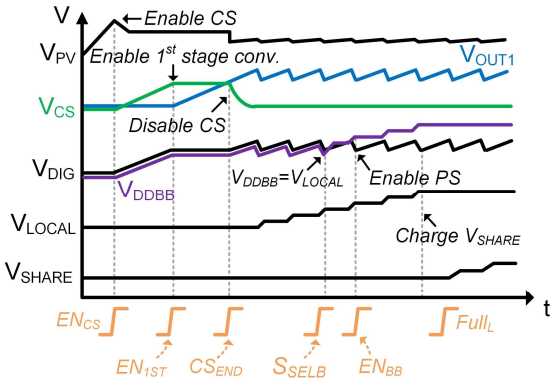

Fig. 16. The timing waveform for the cold startup process.

When EN_{ASYNC} is set to 1, the asynchronous pulse loop is activated. The *DONE* signal is utilized to generate a high frequency asynchronous pulse, as shown in Fig. 15. The asynchronous pulse is then selected to be CLK_{REG} to overclock the comparator and 2nd stage converter, enabling fast rail regulation. Therefore, unlike [33], there is no need to implement any extra high frequency clock, which saves

energy and area. Furthermore, when the V_{SHARE} and V_{LOCAL} rail both are full, the 2nd stage converter cannot effectively extract the surplus energy to regulate the V_{DIG} rail. Therefore, a voltage clamper is enabled to discharge the excessive energy to ground, ensuring that the V_{DIG} rail remains within the desired voltage range.

3) Cold Startup Circuit and Voltage Selector: The cold startup circuits and voltage selectors facilitate the startup process and pick the proper supply voltage for the control circuits. The cold startup circuits include a four-phase voltage doubler and a non-overlapping phase generator [18][37]. By default, as shown in Fig. 12 and Fig. 16, once the V_{PV} reaches above 220 mV, the POR triggers (EN_{CS}=1) and cold startup circuits are enabled to charge the V_{DIG} rail. When the V_{DIG} is charged to 440 mV, the 1st stage converter and related circuits are enabled (EN_{1ST}=1) to charge the V_{OUT1} rail. The voltage selector keeps comparing the V_{OUT1} and V_{CS} rails. When V_{OUT1} is larger than the V_{CS} (V_{DIG}) rail, the voltage selector disables the cold startup circuits (CS_{END}=1) and picks V_{OUT1} as V_{DIG} to power the control circuits. Similarly, once the V_{LOCAL} rail is powered and is larger than the V_{DIG} rail, the voltage selector uses the V_{LOCAL} rail to power the V_{DDBB} (SEL_B=1) rail. When V_{DDBB} reaches 650 mV, the PS control becomes active (EN_{BB}=1). Following this, the EHPMU continues to charge the V_{LOCAL} and V_{SHARE} rails using the algorithm discussed in Section II-B.

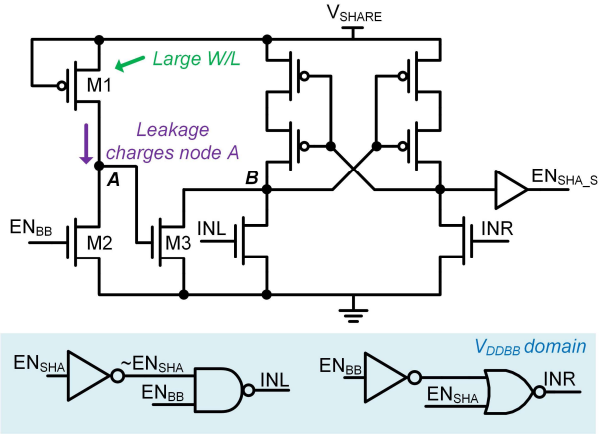

Fig. 17. The schematic of the default high levelshifter.

4) PS Control: The PS control circuits include voltage dividers, an FSM for sharing control, and two hysteresis comparators clocked by a current-starving ring oscillator (CS-OSC) to monitor and manage the V_{LOCAL} and V_{SHARE} rails. Before the chip starts up, the V_{SHARE} and SoC should be disconnected to avoid potential short circuit current at the V_{SHARE} rail or slow startup. On the other hand, the V_{LOCAL} rail should be charged first to power the local components. To achieve this, a back-to-back switch along with a default-high level-shifter is implemented. The back-to-back switch is controlled by two signals, $EN_{SHA,}$ and EN_{SHA_S}, which operate in the V_{DDBB} and V_{SHARE} voltage domains, respectively. A default voltage high levelshifter cuts the connection between the V_{SHARE} rail and SoC, as shown in Fig. 17. Under normal conditions, when the V_{LOCAL} rail does not reach the threshold voltage, the EN_{BB} signal is set low, ensuring that the INL signal is high, and the INR signal is low. However, there are cases where the V_{LOCAL} rail voltage is too low, causing failure of the digital logics and insufficient voltage at INL, which cannot pull node B to ground. This leads to a large short-circuit current and incorrect outputs. To address this issue, M1-M3 transistors are added. When V_{SHARE} is at a high voltage, regardless of the V_{LOCAL}, the leakage current from the M1 transistor charges the node A to turn on the M3 transistor, pulling down the node B to low, which forces the output to be high to disconnect the V_{SHARE} rail.

E. Ripple Boot-up RAM

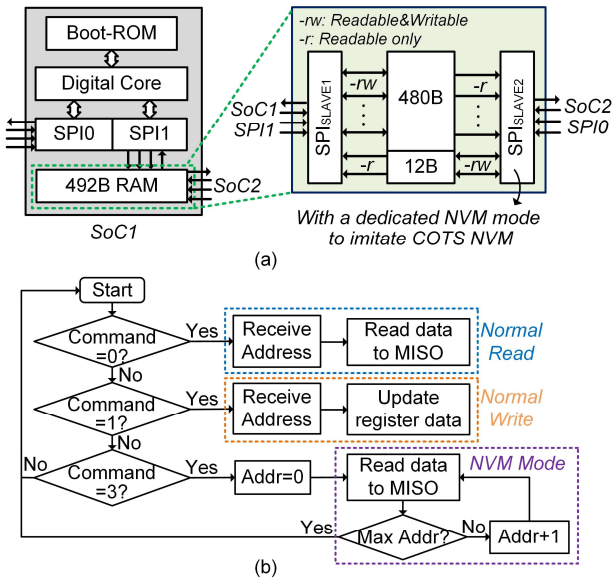

Fig. 18. (a) the schematic and connectivity of the RB-RAM; (b) flow chart of the operating principle for SPI_{SLAVE2}.

The RB-RAM consists of two SPI slaves (SPI_{SLAVE1} and SPI_{SLAVE2}) and a 48-byte flip-flop-based register. The RB-RAM could be synthesized along with the SDLS based digital core and memory-mapped in the address space, but this would impose a large additional area from all the RB-RAM registers due to the large SDLS gate sizes. To avoid this area penalty, the RB-RAM is synthesized with compact traditional static CMOS logic which can be power gated for power saving and connected to the digital core as a SPI slave. Fig. 18 (a) shows the schematic and connectivity of the RB-RAM. The SPI1 connects its local RB-RAM over SPI_{SLAVE1} while the SPI0 is connected to SPI_{SLAVE2} of the neighboring SoCs. All the registers are readable by the two SPI slaves. 12 bytes are writable by the $SPI_{SLAVE2,}$ and the rest are writable by the SPI_{SLAVE1}. To enable the SoC to boot-up from either an NVM or RB-RAM, a NVM mode is added to the SPI_{SLAVE2} to imitate the behavior of the COTS NVM [39], as shown in Fig. 18 (b). Whenever the SoC boots-up from the NVM/RB-RAM, it sends out a command (0x3) and keeps reading all the data stored in the NVM/RB-RAM. By default, the RB-RAM is power gated to save power and allow the SoC to start up in a darker environment.

IV. Experimental Results

The SoC is fabricated in a bulk planar 65nm LP CMOS. The die photo is shown in Fig. 20 with a die area of 3.15 × 2 mm. The two SPI ports and ground pads (VSS) are positioned to the left and right sides for convenient fiber integration.

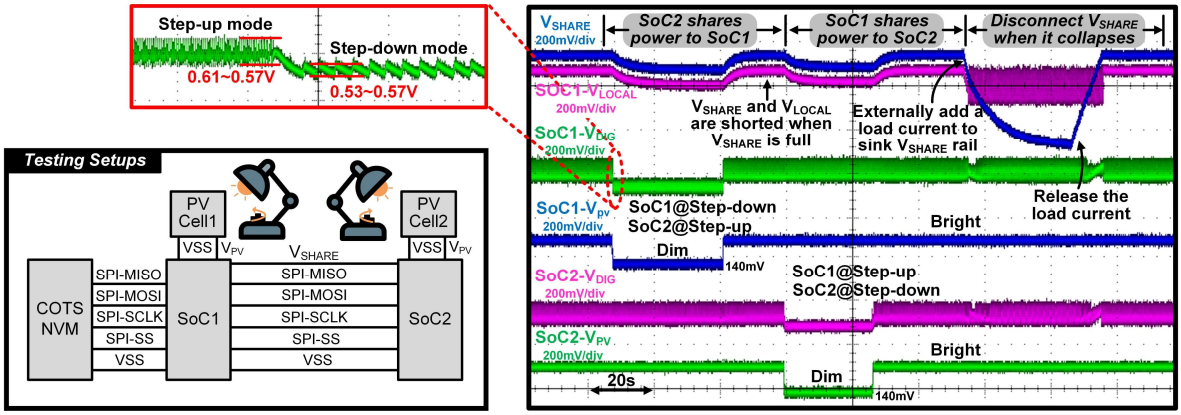

Fig. 19. The testing setup and measured timing waveform of distributed harvesting and PS.

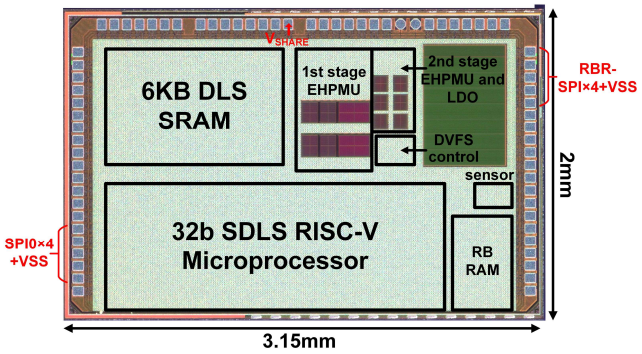

Fig. 20. Chip micrograph of the nanoSiF SoC.

A. Fiber Integration and Fiber Characteristics

The steps of the fiber integration are shown in Fig. 21. The polymer fiber used for integration was thermally drawn from a polyetherimide (PEI) preform with engineered channels. Copper conductor wires were inserted into these channels and incorporated into the fiber, with active feedback control of the wire-pitch. The integration of the SoC onto the fiber was achieved using a post-draw integration process: 1) the top layer of the PEI material is removed to create pockets and expose the copper wires; 2) the wires are cut in the middle; 3) the SoC is wire-bonded onto an interposer which is then soldered onto the exposed wires, followed by encapsulation with UV-cure epoxy.

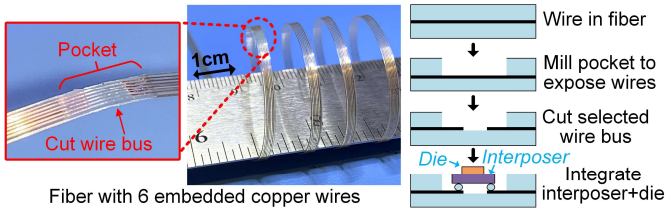

Fig. 21. nanoSiF fiber integration process.

Measured results show that this fiber has a parasitic characteristic of 0.025 ohm/cm, 15.3 nH/cm, and 0.4 pF/cm. These parasitics are inherent to the fiber fabrication process, the spacing between embedded wires, the materials used in the fiber, etc. The maximal speed of the SPI communication between two SoCs and power sharing efficiency would degrade when these parasitic accumulates to a significant value. Since our applications targets on sub-µW and low bandwidth (<1KHz) applications, the impact of these parasitics on the system's functionality and efficiency becomes noticeable when the distance between two SoCs reaches the scale of tens of meters, as per our calculations. For high-speed applications, careful considerations and management of these parasitics become crucial.

B. System-Level Operation: Distributed Harvesting and PS

A benchtop testing setup is shown in Fig. 19, where two SoCs are connected over V_{SHARE}, SPI ports, and ground. A COTS NVM [39] is powered by an external supply and connected to the SoC1 over SPI. The SoCs are tested with CPGA08421 packages. Each of the SoC is paired with a 10 nF input capacitor at V_{PV} rail, a 100 nF capacitor at V_{DIG} rail, a 100 nF capacitor at V_{LDO} rail, and a 1 µF capacitor at V_{LOCAL} rail. A 10 µF capacitor is connected at the shared V_{SHARE} rial. The measured waveform shows that when the environment condition deteriorates, they can configure themselves into step-down mode to utilize the energy from V_{SHARE} rail. While the V_{SHARE} rail is being charged by the other SoC under good lighting conditions. Besides, the two SoCs can isolate V_{LOCAL} from the V_{SHARE} rail when the V_{SHARE} collapses.

C. System-Level Operation: Cold Startup and Ripple Boot-up

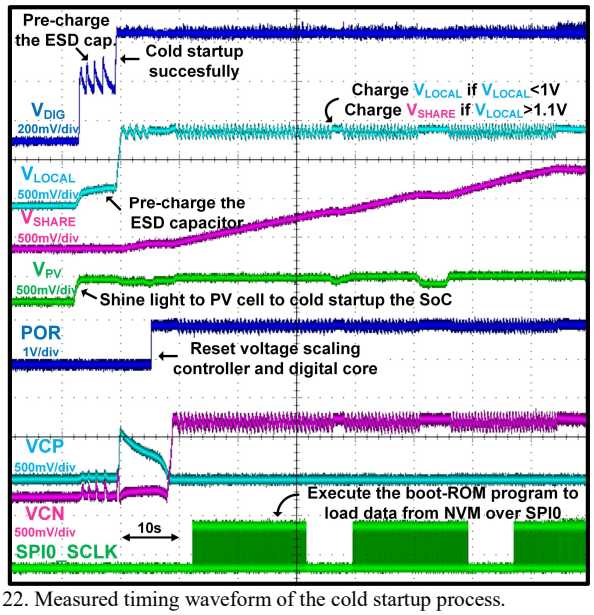

Fig. 22. Measured timing waveform of the cold startup process.

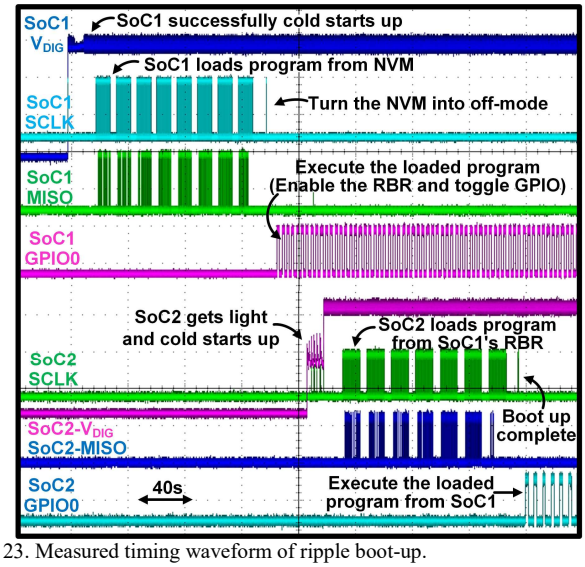

Fig. 23. Measured timing waveform of ripple boot-up.

The measured waveform for cold startup is demonstrated in Fig. 22. When the input V_{PV} reaches 220 mV, the cold startup circuit starts to charge the V_{DIG} rail and the electrostatic discharge (ESD) capacitor at the V_{LOCAL} rail to a certain voltage level. Then the main converters start to charge the V_{LOCAL} and V_{SHARE} rails. Once the V_{LOCAL} rail is full, the system POR triggers. At this point, the V_{CN} and V_{CP} are set to run the core in the fastest mode, and the ACG is enabled, allowing the core to quickly load programs over the SPI0. The measured ripple boot-up waveform shows that SoC1 can cold startup, boot-up from the NVM, and execute the program to activate its RB-RAM. Once SoC2 gets sufficient illumination for cold startup, it boots-up from SoC1 by reading the program stored in the RB-RAM of SoC1 and then executes the loaded program, as shown in Fig. 23.

D. System-Level Operation: Cooperative DVFS

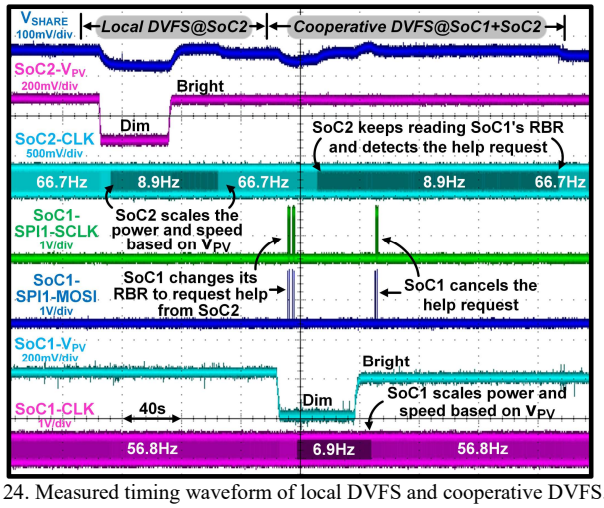

Fig. 24. Measured timing waveform of local DVFS and cooperative DVFS.

The measured cooperative DVFS waveform, as illustrated in Fig. 24, shows the behavior of the two SoCs in response to illumination changes. Once SoC1 enters a dark condition, it changes its RB-RAM value to indicate a help request and then moves into local DVFS mode to slow down to match input energy. SoC2 keeps reading SoC1's RB-RAM value, and when it detects the request, it slows itself down to share more power with the V_{SHARE} rail. Compared with the local DVFS, where only one SoC is dynamically scaling the performance, the cooperative DVFS achieves a faster recovery and reduced voltage fluctuations of the V_{SHARE} rail.

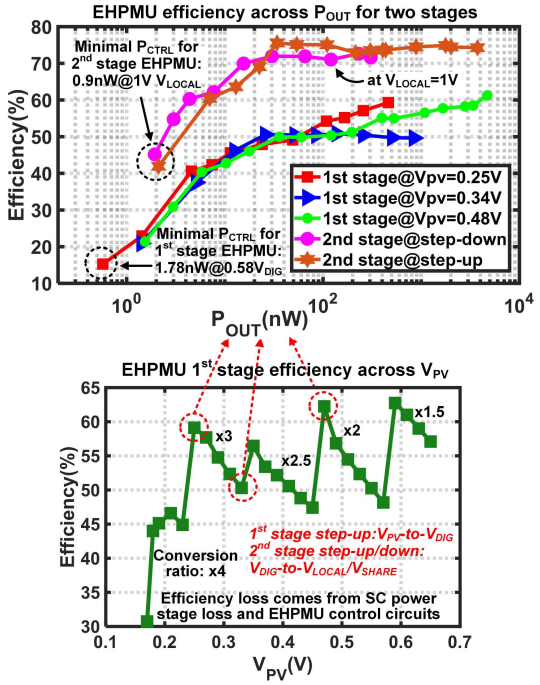

Fig. 25. Measured efficiency vs. output power consumption and input voltage range with different conversion ratios.

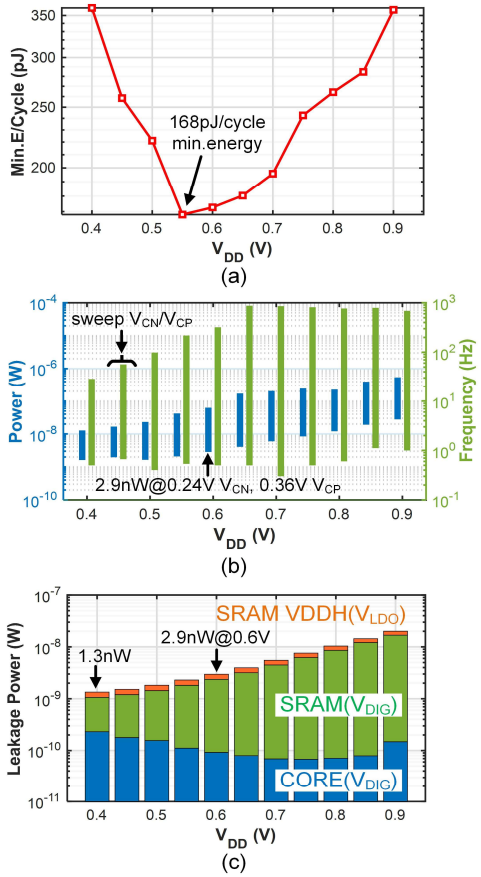

Fig. 26. Measured (a) energy per cycle; (b) performance and power scaling range; (c) leakage power scaling range of the core (RISC-V and SRAM) [18].

Table I: Comparison of the nanoSiF SoC with prior self-powered microsystems and SiFs

	[1] Nature Commu.`21	[2] Nature Commu. 21	[11] RFIC`17	[14] VLSI'18	[15] ISSCC`22	[16] JSSC`22	This Work
Technology	N/R	N/R	65nm	55nm DDC	55nm triple-well	180nm	**65nm**
Sensor	Na^+ Concentration	Temperature	Glucose Concentration	Temperature	Temperature + Electric Field	Neural Recording	**Temperature**
Processor and Memory	ATtiny441**	STM32F401**+24 CW1280X**	No	Arm Cortex M0+ +4Kb SRAM	MCU+480b Mem.	No	**RISCV+6KB SRAM**
Operating Frequency	8MHz* or 32KHz*	4-26MHz* or 32KHz*	0.1-2MHz @Recovered Clock	48Hz or Recovered Clock	N/R	350-1080Hz BW @40Hz LED Firing	**<850Hz**
Self-Powered	Yes, TEG/BFC	No	Yes, PV	Yes, PV	Yes, PV	Yes, PV	**Yes, PV**
Distributed Energy Harvesting	No	No	No	No	No	No	**Yes**
Power Sharing	No	No	No	No	No	No	**Yes**
Cold Startup	Yes	N/R	Yes	Yes	Yes	Yes	**Yes**
Boot-up Function	No, preprogram	Yes	No	Yes	Yes	No	**Yes, Ripple Boot-up**
Communication	Yes	Yes, Wireline	Yes, RF/Optical	Yes, Optical	Yes, Optical/Move	Yes, Optical	**Yes, Wireline**
Cooperative DVFS	No	No	No	No	No	No	**Yes**
Minimal System Power	4mW@2V	5.78μW@1.7V, standby*	63nW	16nW	75nW@60Klux	570nW (38°C)	**33nW@0.183V V_{PV} (92Lux)**
Components included in System Power	MCU** +PMU**+sensor+ ECD+IO	MCU**+ EEPROM**+ Sensor**	CLK+Current Reference+PMU	MCU+SRAM+ ROM+CLK+PMU+ sensor+TRx	MCU+SRAM+ROM+ Sensor+CLK+Rx	AFE+Rx+CLK+ Bias	**Full Chip: Sensor+MCU+ SRAM+ROM+CLK+EHPMU +ESD+IO+V_{CN},V_{CP} Gen.**
PMU Topology	Inductor	No, Battery	SC	SC	No, EH only	No, EH only	**SC+LDO**
PMU Peak Efficiency (%)	N/R	No	46%@100nA I_{load}	N/R	N/R	N/R	**62.7%@1st stage 74.8%@2nd stage-Boost 72.6%@2nd stage-Buck**
System Integration	E-texile with films	Embedded in fiber thread	TSV to back side of IC	Stacked with bond wire	Monolithic fabricated robot	Stacked with flip chip	**Embedded in fiber with interposer and bond wires**
Device Size	>1cm^3*	840x900x400µm	200x200x100µm	360x400x280µm	210×340×50µm	190x280µm	**4.7×3.7mm interposer on a 2.2×1mm cross-section fiber**
Minimal V_{IN}/Lux for system survival	0.33V	1.7V*	N/R	3Klux	60Klux	N/R	**180mV(90Lux)@Single SoC 145mV(12Lux)@Power Share**

*Calculated from the paper
**Commercial off-the-shelf products

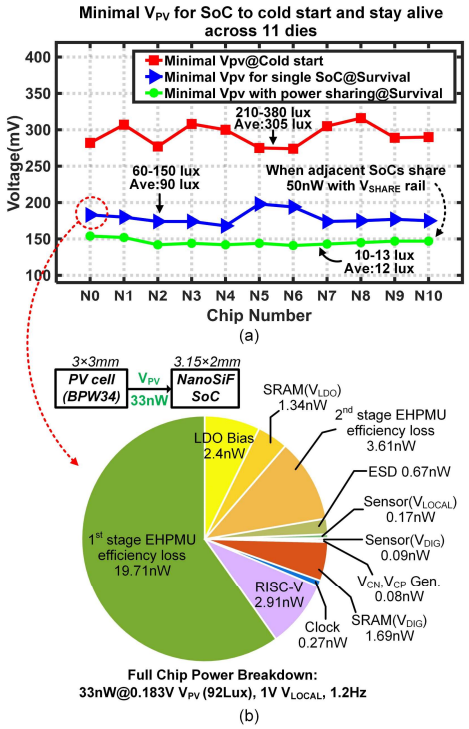

Fig. 27. (a) measured minimal input voltage / Lux for the SoC to cold startup and stay alive with/without power sharing; (b) measured full chip power breakdown at 0.183 V V_{PV} under 92 Lux with a 3×3 mm PV cell.

E. EHPMU Efficiency

Fig. 25 shows the measured efficiency for the EHPMU across output power (P_{OUT}) and V_{PV} with different conversion ratios. The EHPMU achieves a 62.7% peak efficiency for the 1st stage converter at conversion ratio of 1.5×. It also achieves 74.8% and 72.6% peak efficiency for 2nd stage converter in step-up and step-down mode, respectively, with a 2.7 nW minimum control power (1.78 nW and 0.9 nW). Moreover, the EHPMU can support a $>3\times10^3$ and $>1\times10^3$ output power range for the 1st and 2nd stage converters, respectively.

F. System Power Consumption and Performance

Fig. 26 provides measurements of the performance, power consumption, leakage scaling range, and energy per cycle of the digital core [18] by manually sweeping V_{DIG} (VDD), V_{CN}, and V_{CP}. The SRAM VDDH is set to V_{DIG} + 0.32 V. The energy per cycle achieves a minimum of 168 pJ/cycle with a power range of 1.3 nW to 511 nW. This demonstrates a 393× power scaling range and an 850 Hz maximal frequency clock. At the nominal voltage of 0.6 V, the core can scale down to 3 nW and up to a maximum of 62 nW at 320 Hz.

Additionally, 11 dies are measured with two BPW34 solar cells [40], one for V_{OC} measurement and one for harvesting. The averaged minimum voltage/Lux required to cold start the SoC is 295 mV / 305 Lux, and the averaged minimum voltage/Lux for the SoC to stay alive is 180 mV / 90 Lux, as shown in Fig. 27 (a). Moreover, when two SoCs are connected (same as the setup in Fig. 19) and one of the SoCs is in a good lighting conditions to share a 50 nW power with the V_{SHARE} rail at 1V, the required minimum Lux for the other SoC to stay alive can be decreased by over 7× down to 12 Lux with the proposed PS. For a single SoC, at the poorest harvesting point (92 Lux), as shown in Fig. 27 (b), the power breakdown for the whole chip achieves a minimum of 33 nW power consumption from the harvesting solar cell while the SoC

keeps reading the temperature sensor data and toggling one of the GPIO pins with a 1.2Hz clock frequency. The temperature sensors functionality is verified and demonstrated in our previous work [18] that the SoC can keep reading and monitoring the temperature, making it well-suited for healthcare applications. Moreover, the design allows for the integration of other fully-integrated ULP sensors, enabling the collection of a broader range of physiological signals.

G. Comparison to state-of-the-art

Table I compares the proposed nanoSiF SoC with state-of-the-art self-powered miniaturized microsystems and SiF. The prior SiF systems [1][2] utilized COTS components, leading to a large power consumption and physical volume. In contrast, the proposed nanoSiF with customized SoCs achieves mm-scale size and full autonomy. With the EHPMU, the SoC enables distributed energy harvesting and multi-chip PS, allowing the SoC to operate in significantly darker environments (>7× darker). These features enable the SoC to maintain continuous sensing under the poorest of lighting conditions. Thanks to the proposed RB-RAM, the SoCs in-fiber can boot-up and communicate with each other, which is not supported by previous microsystems [11][14]-[16]. Integrated into a 2.2×1 mm cross-section fiber strand with a 4.7×3.7 mm interposer, the SoC is shown to be compatible with the post-draw integration technique for fiber integration.

V. Discussion and Future Work

To truly enable a robust, self-powered, and intelligent SiF system and expedite its commercialization, this work presents opportunities for future innovations and improvements to overcome existing limitations. In the current architecture, the SoCs can only directly interact with the up/downstream SoCs resulting in a dependence on the upstream SoCs for downstream SoC boot-up. If SoCs in the middle of the fiber are non-functional, the downstream SoCs cannot boot-up successfully due to this dependence. This limitation could be addressed through three potential solutions that merit exploration. One approach is to implement a periodical detection function in each SoC to check whether the upstream SoC is ready. Another solution is to add a "ready" signal sent from upstream SoC so that the downstream SoC boots-up once the upstream SoC is ready. The third approach is to add an extra function to allow the SoCs to bypass or skip these "dead" SoCs in between, empowering the SoCs with a more flexible communication capability. Moreover, future research could focus on developing new ULP protocols [41] or topologies (e.g., with extra coordinated chips) to enable flexible communication for SiF applications. Besides, other types of ULP fully-integrated sensors, nW-level MCU with wider dynamic ranges for high-bandwidth applications, and fiber fabrication technology with less parasitics can be further developed to unlock the full potential of SiF system for a multitude of applications in healthcare and beyond.

VI. Conclusion

In this work, we present a self-powered SoC with distributed energy harvesting and cooperative multi-chip power management for SiF. The proposed SoC addresses the limitations of existing systems through autonomous operation, miniaturization, continuous sensing at nW-level power consumption, and direct inter-SoC communication in a distributed sensing network.

The key features of the proposed SoC include distributed energy harvesting, PS, (S)DLS technology based digital core and sensor, ripple boot-up, and cooperative DVFS. These features enable the SoCs to operate autonomously, cooperatively balance energy and performance among adjacent SoCs in-fiber and improve the utilization of harvested energy along the fiber. Fabricated in a 65 nm technology and validated with miniature solar cells, these technologies significantly reduce the power consumption of the whole chip down to 33 nW and allow continuous sensing under the lowest lighting conditions (90 Lux), compared with prior art. Moreover, with those techniques, the SoC can operate in a >7x darker environment down to 12 Lux by cooperating with neighboring SoCs. These features and experimental results contribute to the realization of fully autonomous, miniaturized, and adaptable SiF applications, making our SoC well-suited for ULP SiF applications in various domains.

References

[1] Yin, L., Kim, K.N., Lv, J. et al. "A self-sustainable wearable multi-modular E-textile bioenergy microgrid system", *Nature Comm.*, vol. 12, issue 1, pp. 1542–1553, Mar. 2021.

[2] G. Loke et al., "Digital Electronics in Fibres Enable Fabric-Based Machine-Learning Inference," *Nature Comm.*, vol. 12, pp. 3317–3325, Jun. 2021.

[3] Chen, M., Wang, Z., Zhang, Q. et al. "Self-powered multifunctional sensing based on super-elastic fibers by soluble-core thermal drawing," *Nature Comm.*, vol. 12, issue 1, pp. 1416–1425, Mar. 2021.

[4] Hwang, S., Kang, M., Lee, A. et al. "Integration of multiple electronic components on a microfibre towards an emerging electronic textile platform", *Nature Comm.*, vol. 13, issue 1, no. 3173–3182, Jun. 2022.

[5] Kim, J., Campbell, A.S., de Ávila, B.EF. et al. "Wearable biosensors for healthcare monitoring", *Nature Biotech.*, vol. 37, issue 4, pp. 389-406, Apr. 2019.

[6] Wicaksono, I., Tucker, C.I., Sun, T. et al. "A tailored, electronic textile conformable suit for large-scale spatiotemporal physiological sensing in vivo", *npj Flex Electron,* vol. 4, issue 1, pp. 5–17, Apr. 2020.

[7] 1MC04-serial TEG, TEC microsystem. Accessed: May 26, 2023. [Online]. Available: https://www.tec-microsystems.com/products/thermoelectric-generators/

[8] Jingjing Tian et al., "Self-powered implantable electrical stimulator for osteoblasts' proliferation and differentiation", *Nano Energy*, vol. 59, pp. 705-714, May 2019.

[9] D. Cabello et al., "On-Chip Solar Energy Harvester and PMU With Cold Start-Up and Regulated Output Voltage for Biomedical Applications," *IEEE Trans. on Circuits and Syst. I, Reg. Papers*, vol. 67, no. 4, pp. 1103-1114, April 2020.

[10] Chakravarti A et al., "Wireless Photometry Prototype for Tri-Color Excitation and Multi-Region Recording. Micromachines," *Micromachines*, vol. 13, no. 5, Apr. 2022.

[11] S. O'Driscoll et al., "A 200µm × 200µm × 100µm, 63nW, 2.4GHz injectable fully monolithic wireless bio-sensing system," in *IEEE RFIC*, Honolulu, HI, USA, 2017, pp. 256-259.

[12] Zhongyang Ren et al., "Wearable and self-cleaning hybrid energy harvesting system based on micro/nanostructured haze film," *Nano Energy*, vol. 67, pp. 104-243, 2020.

[13] DigiKey Catalog of Off-the-Shelf Components. Accessed: May. 26, 2023. [Online]. Available: https://www.digikey.com

[14] X. Wu et al., "A 0.04mm^3 16nW Wireless and Batteryless Sensor System with Integrated Cortex-M0+ Processor and Optical Communication for Cellular Temperature Measurement," in *IEEE Symp. VLSI Circuits Dig.*, Honolulu, HI, USA, 2018, pp. 191-192.

[15] L. Xu et al., "A 210×340×50µm Integrated CMOS System for Micro-Robots with Energy Harvesting, Sensing, Processing, Communication and

Actuation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, 2022, pp. 1-3.
[16]J. Lim et al., "A Light-Tolerant Wireless Neural Recording IC for Motor Prediction with Near-Infrared-Based Power and Data Telemetry," *IEEE J. Solid-State Circuits*, vol. 57, no. 4, pp. 1061-1074, April 2022.
[17]S. Li, X. Liu and B. H. Calhoun, "A 32nA Fully Autonomous Multi-Input Single-Inductor Multi-Output Energy-Harvesting and Power-Management Platform with 1.2×105 Dynamic Range, Integrated MPPT, and Multi-Modal Cold Start-Up," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, 2022, pp. 1-3.
[18]D. Truesdell et al., "NanoWattch: A Self-Powered 3-nW RISC-V SoC Operable from 160mV Photovoltaic Input with Integrated Temperature Sensing and Adaptive Performance Scaling," in *IEEE Symp. VLSI Circuits Dig.*, pp. 210-211, June 2022.
[19]X. Liu et al., "A Self-Powered SoC with Distributed Cooperative Energy Harvesting and Multi-Chip Power Management for System-in-Fiber," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, 2023, pp. 236-238.
[20]L. Lin et al., "Sub-nW Microcontroller with Dual-Mode Logic and Self-Startup for Battery-Indifferent Sensor Nodes," *IEEE J. Solid-State Circuits*, vol. 56, no. 5, pp. 1618-1629, May 2021.
[21]P. A. Meinerzhagen et al., "An Energy-Efficient Graphics Processor in 14- nm Tri-Gate CMOS Featuring Integrated Voltage Regulators for Fine Grain DVFS, Retentive Sleep, and V_{MIN} Optimization," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 144-157, Jan. 2019
[22]X. Liu et al., "A 194nW Energy-Performance-Aware loT SoC Employing a 5.2nW 92.6% Peak Efficiency Power Management Unit for System Performance Scaling, Fast DVFS and Energy Minimization," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 224-225, Feb. 2022.
[23]C. J. Lukas et al., "A 1.02 µW Battery-Less, Continuous Sensing and Post-Processing SiP for Wearable Applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 2, pp. 271-281, April 2019.
[24]D. Bol et al., "SleepRunner: A 28-nm FDSOI ULP Cortex-M0 MCU With ULL SRAM and UFBR PVT Compensation for 2.6–3.6-µW/DMIPS 40–80-MHz Active Mode and 131-nW/kB Fully Retentive Deep-Sleep Mode," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2256-2269, July 2021.
[25]J. Myers et al., "A 12.4pJ/cycle sub-threshold, 16pJ/cycle near-threshold ARM Cortex-M0+ MCU with autonomous SRPG/DVFS and temperature tracking clocks," in *IEEE Symp. VLSI Circuits Dig.*, 2017, pp. C332-C333.
[26]W. Lim, I. Lee, D. Sylvester, and D. Blaauw, "Batteryless sub-nW cortexM0+ processor with dynamic leakage-suppression logic," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, 2015, pp. 1–3.
[27]D. S. Truesdell, J. Breiholz, S. Kamineni, N. Liu, A. Magyar and B. H. Calhoun, "A 6–140-nW 11 Hz–8.2-kHz DVFS RISC-V Microprocessor Using Scalable Dynamic Leakage-Suppression Logic," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 8, pp. 57-60, Aug. 2019.
[28]S. Gupta, D. S. Truesdell and B. H. Calhoun, "A 65nm 16kb SRAM with 131.5pW Leakage at 0.9V for Wireless IoT Sensor Nodes," in *IEEE Symp. VLSI Circuits Dig.*, Honolulu, HI, USA, 2020, pp. 1-2.
[29]D. Truesdell and B. H. Calhoun, "A 640 pW 22 pJ/sample Gate Leakage-Based Digital CMOS Temperature Sensor with 0.25°C Resolution," *in Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, pp. 1-4, Apr. 2019.
[30]K. A. et al., "The rocket chip generator," *Dept. Elect. Eng. Comput. Sci., Univ. California, Berkeley*, vol. Tech. Rep. UCB/EECS-2016-17, 2011.
[31]S. Carreon-Bautista et al., "An Autonomous Energy Harvesting Power Management Unit with Digital Regulation for IoT Applications," *IEEE J. Solid-State Circuits*, vol. 51, no. 6, pp. 1457- 1474, June 2016.
[32]J. Li, et al., "Triple-Mode, Hybrid-Storage, Energy Harvesting Power Management Unit: Achieving High Efficiency Against Harvesting and Load Power Variabilities," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2550-2562, Oct. 2017.
[33]H. Kim et al., "A Dual-Mode Continuously Scalable-Conversion-Ratio SC Energy Harvesting Interface With SC-Based PFM MPPT and Flying Capacitor Sharing Scheme," *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2724-2735, Sept. 2021.
[34]H. -C. Cheng, P. -H. Chen, Y. -T. Su and P. -H. Chen, "A Reconfigurable Capacitive Power Converter with Capacitance Redistribution for Indoor Light-Powered Batteryless Internet-of-Things Devices," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 2934-2942, Oct. 2021.
[35]K. Rawy, T. Yoo and T. T. -H. Kim, "An 88% Efficiency 0.1–300- µ W Energy Harvesting System With 3-D MPPT Using Switch Width Modulation for IoT Smart Nodes," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2751-2762, Oct. 2018.
[36]M. -K. Law, Y. Jiang, P. -I. Mak and R. P. Martins, "Miniaturized Energy Harvesting Systems Using Switched-Capacitor DC-DC Converters," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 69, no. 6, pp. 2629-2634, June 2022.
[37]X. Liu, B. H. Calhoun, and S. Li, "A Sub-nW 93% Peak Efficiency Buck Converter with Wide Dynamic Range, Fast DVFS, and Asynchronous Load-Transient Control," *IEEE J. Solid-State Circuits*, vol. 57, no. 7, pp. 2054-2067, July 2022.
[38]T. Ozaki, T. Hirose, T. Nagai, K. Tsubaki, N. Kuroki and M. Numa, "A 0.21-V minimum input, 73.6% maximum efficiency, fully integrated voltage boost converter with MPPT for low-voltage energy harvesters," *in Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, Venice Lido, Italy, 2014, pp. 255-258.
[39]RM25C32DS, Adesto technology. Accessed: May 26, 2023. [Online]. Available: https://www.mouser.com/datasheet/2/590/RM25C32DS_124-1385829.pdf
[40]Miniature Solar Cell, SparkFun. Accessed: May 26, 2023. [Online]. Available: https://www.mouser.com/c/power/solar-panels-solar-cells/?m=SparkFun%20Electronics
[41]Y. -s. Kuo et al., "MBus: A 17.5 pJ/bit/chip portable interconnect bus for millimeter-scale sensor systems with 8 nW standby power," *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, USA, 2014, pp. 1-4.

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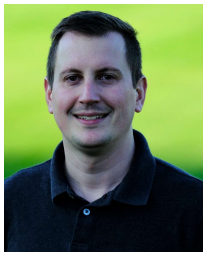

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