An 802pW 93% Peak Efficiency Buck Converter with 5.5×10^6 Dynamic Range Featuring Fast DVFS and Asynchronous Load-Transient Control

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***Abstract*—This paper presents a buck converter with sub-nW quiescent power, high efficiency, and a wide dynamic range for ultra-low-power (ULP) IoT SoCs. To optimize the SoC power consumption, the buck converter supports fast dynamic voltage and frequency scaling (DVFS) and enables fast load-transient response (FLTR) through asynchronous control. In addition, the buck converter is fully self-contained with all features integrated on chip including a proposed adaptive deadtime controller. Fabricated in 65nm CMOS, measurement results show the buck converter has an 802pW quiescent power at 1.5V input voltage and a 93% peak efficiency. The measured dynamic range is from 0.5nW to 2.75mW, which is over 6 orders of magnitude. The measured voltage droop is 54mV for a 45nA-to-1mA load current step thanks to the asynchronous load-transient detector. The buck converter achieves the highest efficiency and widest dynamic range among all the state-of-the-art sub-nW switching voltage regulators, which makes it well suited for power management in ULP SoCs.**

Keywords—buck converter, sub-nW quiescent power, wide dynamic range, high efficiency, fast DVFS, asynchronous control, fast load-transient response

I. Introduction

Power scaling of IoT SoCs from mW down to μW and nW enables the capability of energy harvesting and minimizes the form factor due to smaller energy store node. Recent IoT chips already achieve active power in a few nW or even pW range [1]. To optimize the SoC power and performance, several techniques have been widely used including dynamic voltage and frequency scaling (DVFS) and duty-cycling control. However, the power scaling trend brings many challenges to the power delivery circuitry. Especially, designing a DC-DC converter with high power efficiency and wide dynamic range down to nW level while supporting fast DVFS and duty-cycled loads is becoming critical for this application space.

Achieving high efficiency for nW output power requires voltage regulators to have sub-nW quiescent power. The previous sub-nA digital low dropout regulator (LDO) [2] can achieve a wide dynamic range and fast transient response, but the power efficiency is low for a large input and output voltage ratio. Switched-capacitor DC-DC converters [3] can also achieve very low quiescent power, but suffer from poor efficiency and small dynamic range. Inductor-based switching voltage regulators can provide a high efficiency for a large dynamic range, which are widely adopted as the first power-delivery stage. However, the previous sub-nW switching voltage converters [4] [5] do not support DVFS and fast load-transient response (FLTR). To enable DVFS and FLTR, traditional voltage regulators [6] use high frequency clock (>1MHz), which consumes too much power and makes them not suitable for ultra-low-power (ULP) IoT applications, and voltage regulators with low quiescent power cannot achieve fast response due to limited loop bandwidth using traditional synchronous feedback control.

In this work, we present a sub-nW buck converter with a high efficiency and wide dynamic range for ULP IoT applications. The buck converter also enables an on-chip fast DVFS and FLTR using asynchronous feedback. Fabricated in 65nm CMOS, this buck converter achieves 802pW quiescent power at 1.5V input voltage and a 93.1% peak efficiency. It also has a dynamic range of 5.5×10^6 from 0.5nW to 2.75mW. The measured DVFS speed is 6μs/50mV and 10.76μs/50mV for up and down tracking separately, and the measured voltage droop is 54mV for a 45nA-to-1mA load current step.

II. System Architecture and Implementations

A. System Overview

The block diagram of the proposed buck converter is shown in Fig. 1, which consists of a power stage, high-side (HS) and low-side (LS) pulse generators, an adaptive deadtime controller, a zero-current detector (ZCD), a hybrid pulse-frequency control block, an adjustable bias generator, and a power-on reset (POR). During general operation, the strong-ARM latch, LATH, compares V_{OUT} with V_{REF} to generate the control signal, EN_{BUCK}, and enable power delivery under discontinuous-conduction mode (DCM). After a complete power delivery phase, the ZCD comparator compares the switching node, SWD, with V_{SS} and adjusts the LS pulse width through a counter to achieve zero-current switching (ZCS).

To reduce the quiescent power down to sub-nW, several techniques have been adopted in this work. First, an energy-efficient current-starved ring oscillator (CS-OSC) is used to generate a frequency range down to tens of Hz, which minimizes the power consumption of the system. Second, a length modulation scheme in the power stage reduces the leakage and increases the efficiency for nW output power and gate drivers has been optimized by using a strong pull-up and weak pull-down (SuWd) scheme to reduce the leakage while maintaining a high efficiency for power delivery. Finally, a

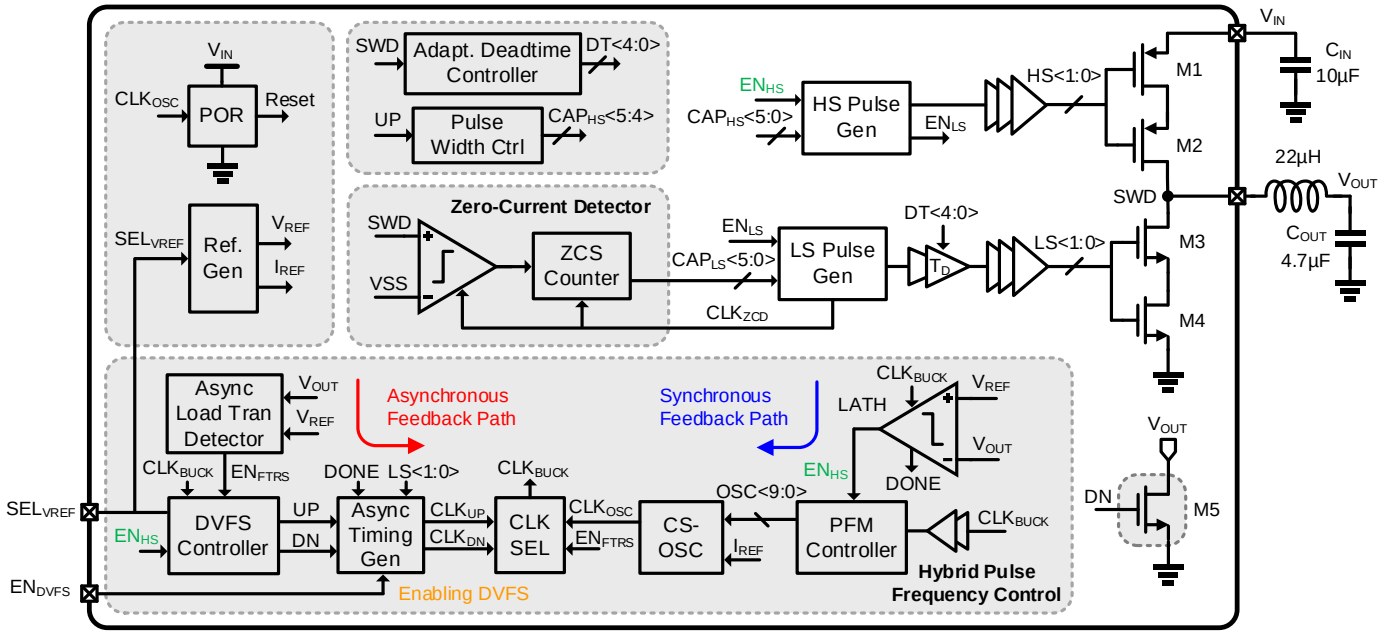

Fig. 1. System block diagram of the proposed sub-nW buck converter.

digital ZCD which only consumes leakage quiescent power is used to replace the traditional power-hungry analog ZCD.

Ultra-low quiescent power usually reduces loop bandwidth and speed. To keep sub-nW power while maintain a fast transient-response, a hybrid pulse-frequency control scheme has been proposed, including a synchronous (sync) feedback for general voltage regulation and an asynchronous (async) feedback for FLTR and fast DVFS. By using the hybrid control scheme, the buck converter supports fast DVFS and FLTR with only sub-nW quiescent power consumption. It also includes a pulse width control which generates the largest pulse width during load-transient response or reference up-tracking. This buck converter integrates all the features on chip including a digitally adjustable voltage reference, a POR, and an adaptive deadtime controller.

B. Fast Reference Tracking for DVFS

To support fast DVFS, a reference tracking scheme is implemented using the async feedback and triggered by a load processor. The buck converter output is used to power the processor and a voltage-scaled oscillator. By changing the output voltage, the system can achieve voltage and frequency scaling simultaneously. A DVFS controller monitors the reference selection signal, SEL_{VREF}, using a DVFS enable signal, EN_{DVFS}, and outputs UP or DN signal to start the async reference tracking process.

Fig. 2 shows the waveform of the reference up-tracking. Once enabled by EN_{DVFS} and UP = 1, CLK_{UP} is selected as the buck clock and LS falling edge triggers a pulse, T_P, after a time delay, T_N, to generate CLK_{UP}. The async clock continuously enables power delivery to the output to increase the voltage value until EN_{HS} goes to 0, indicating $V_{OUT} > V_{REF}$. Then it stops the up-tracking and the buck clock, CLK_{BUCK}, switches from CLK_{UP} back to CLK_{OSC}. To regulate the output with a higher V_{REF}, the CLK_{OSC} frequency is set to be maximum after

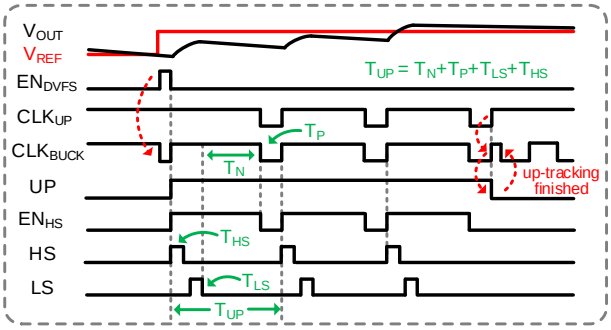

Fig. 2. Operation timing diagram of the reference up-tracking.

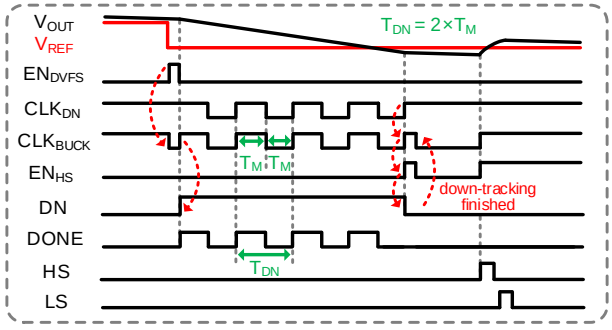

Fig. 3. Operation timing diagram of the reference down-tracking.

the up-tracking process completes. The async clock period is decided by the HS pulse width (T_{HS}), LS pulse width (T_{LS}), T_N, and T_P. Fig. 3 shows the waveform of the down-tracking. Once triggered by EN_{DVFS} and DN = 1, DN turns on the transistor, M_5, to generate a current sink from output to quickly decrease the output voltage. The DONE signal generated by the LATH is used as an indicator to continuously monitor V_{OUT}. The rising edge of the DONE signal followed by a delay (T_M) is used to enable next comparison until EN_{HS} = 1, meaning $V_{OUT} < V_{REF}$. Then, the down-tracking stops and the buck clock

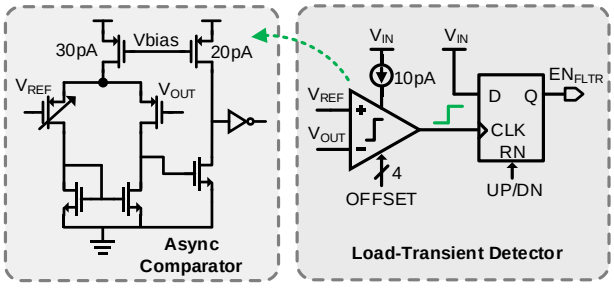

Fig. 4. Schematic of the async load-transient detector.

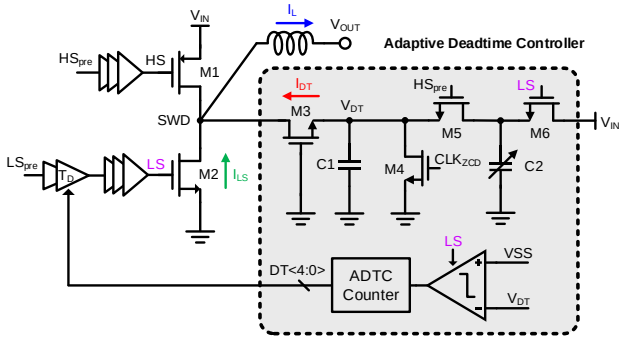

Fig. 5. Schematic of the proposed adaptive deadtime controller.

switches to the CLK_{OSC} again. During down-tracking, the async clock period is equal to $2\times T_M$.

C. *Fast Load-Transient Response*

Fig. 4 shows the schematic of the async load-transient detector, which consists of an async comparator and a D Flip-Flop to sample the FLTR enable signal, EN_{FLTR}. The async comparator uses an amplifier-based structure with 50pA bias current including a 4-bit offset tuning to generate a guardband, ΔV_{GB}. Whenever there is a load step current and V_{OUT} drops below $V_{REF} - \Delta V_{GB}$, the async comparator triggers EN_{FLTR} immediately. After the DVFS controller receives $EN_{FLTR} = 1$, the buck clock is switched to CLK_{UP} through the async feedback path and the transient waveform is similar to the reference up-tracking shown in Fig. 2. The reuse of reference up-tracking blocks with FLTR helps reduce the power and area overhead. The transient response time is dominated by the async comparator delay and the voltage droop depends on the guardband size.

D. *Adaptive Deadtime Controller*

Switching voltage regulators need deadtime between HS and LS pulses to prevent short-circuit current, which also needs to be minimized to reduce the power loss. In this buck converter, we propose an adaptive deadtime controller (ADTC) shown in Fig. 5, which consists of a switched-capacitor based pre-charger, a comparator and a digital counter. The V_{DT} node is first pre-charged to a fixed voltage and during deadtime, to maintain the inductor current, I_L, the voltage at SWD reduces from V_{IN} to a negative voltage to generate I_{LS}. Adding a small size of transistor M3 in parallel with M2 generates a small current I_{DT}, which discharges a capacitor, C1. The time that needs to discharge V_{DT} to V_{SS} through I_{DT} is the designed deadtime. In this design, M2 and M3 keep the same length but

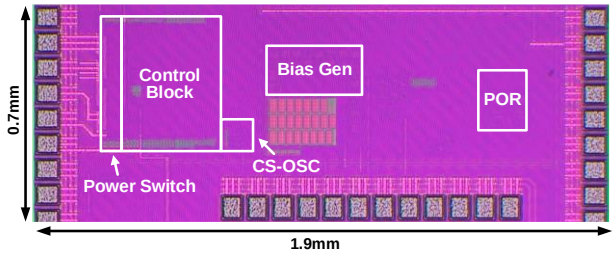

Fig. 6. Chip micrograph of the buck converter.

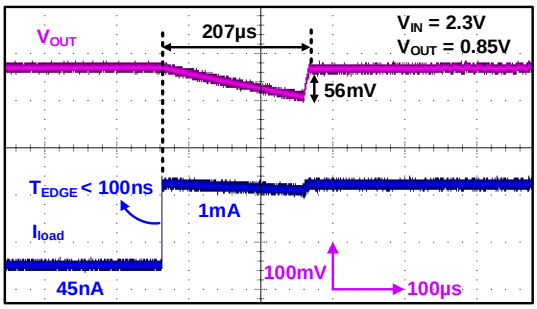

Fig. 7. Measured transient waveform for fast load-transient response.

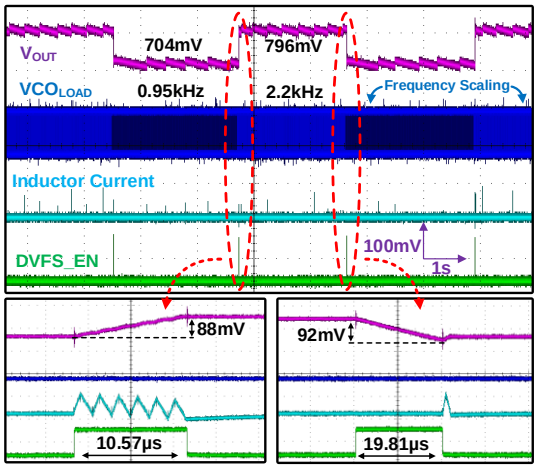

Fig. 8. Measured transient waveform for DVFS up and down tracking.

the width of M3 is 1/375 of M2 making I_{DT} equal to $I_{LS}/375$. By setting proper C1 and C2 values, the deadtime can be adaptively tuned by the ADTC through the delay cell, T_D.

III. Measurement Results

The sub-nW buck converter is fabricated in 65nm CMOS technology with an active area of 0.237mm^2. Fig. 6 shows the chip micrograph of the buck converter.

The measured load-transient response is shown in Fig. 7. When load step current changes from 45nA to 1mA, the voltage droop is 56mV and the settling time is 207µs with a 4.7µF off-chip output capacitor. The measured DVFS tracking waveform is shown in Fig. 8, which achieves 10.57µs for a 88mV up-tracking step and 19.81µs for a 92mV down-tracking step. Without the fast DVFS function, the measured up/down tracking time increases up to 0.93s and 2.65s, respectively. A ring oscillator for digital loads is used in the testing to show the frequency scaling ability. As voltage supply scales down, the

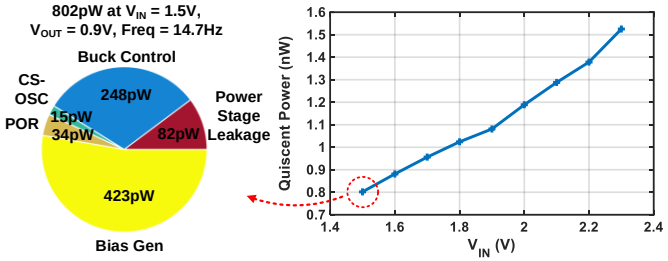

Fig. 9. Measured quiescent power vs V_{IN} and power breakdown at V_{IN} = 1.5V.

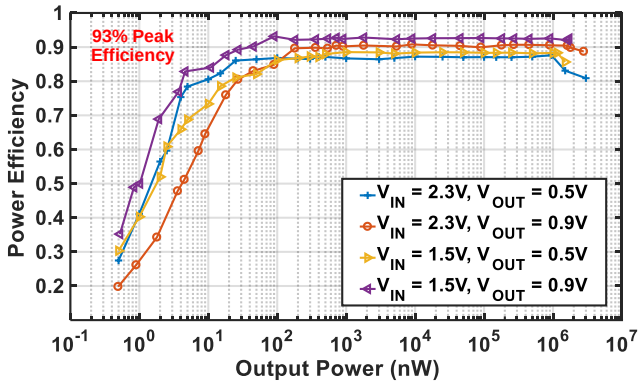

Fig. 10. Measured power efficiency across different V_{IN} and V_{OUT}.

frequency of ring oscillator powered by the buck converter also decreases from 2.2kHz to 0.95kHz. The undershoot and overshoot voltage is less than 4mV which is only 0.5% of V_{OUT} at 700mV and is close to the measured 10mV ripple voltage.

The quiescent power of the buck converter is measured when there is no output power and the clock frequency is at its lowest value, 14.7Hz. Fig. 9 shows the measured quiescent power across different V_{IN}. At 1.5V V_{IN}, the quiescent power is 802pW and the left pie chart shows the detailed power breakdown of the buck converter. Fig. 10 shows the measured power efficiency across different V_{IN} and V_{OUT} with the peak efficiency up to 93%. The buck converter also has a measured dynamic range from 0.5nW to 2.75mW, which provides an over 6 orders of magnitude range and keeps an 80% efficiency even at 4.3nW output power at 1.5V V_{IN} and 0.9V V_{OUT}.

Table I compares this work with state-of-the-art inductor-based pW-nW DC-DC converters. As we can see, our buck converter achieves the highest peak efficiency and widest dynamic range among all the sub-nW switching voltage regulators. The buck converter also supports fast DVFS and fast load-transient response with a 10× improvement on the settling time thanks to the hybrid pulse-frequency control scheme. In addition, the buck converter integrates all the features on chip including a proposed adaptive deadtime controller. All the measured performance and integrated features make the buck converter well suited as the power management solution for ULP IoT applications.

IV. Conclusions

To achieve a high efficiency and wide dynamic range while supporting fast DVFS and load-transient response, we presented a sub-nW buck converter with hybrid synchronous and asynchronous pulse-frequency control. The measurement results show this buck converter achieves an 802pW quiescent power at 1.5V V_{IN}, 93% peak efficiency, 5.5×10^6 dynamic range, and 54mV voltage droop for a 45nA-to-1mA load current step. This buck converter provides an optimal power management solution for ULP IoT SoCs.

TABLE I: Comparison with State-of-the-art pW-nW Inductor-Based DC-DC Converters

	[4] ISSCC'14	[7] JSSC'16	[5] ISSCC'17	[8] JSSC'18	This Work
Technology (nm)	180	130	65	65	**65**
Topology	Boost	Buck-Boost	Buck	Boost	**Buck**
Regulation Scheme	PWM	PFM	PFM	PFM	**PFM/LM/PWM**
L (µH) / C_{OUT} (µF)	47/0.2	47/NR	47/0.35	47/1	**22/4.7**
V_{IN} (V)	0.02-0.07	2.9-4.1	1.2-3.3	0.08-0.8*	**1.4-2.5**
V_{OUT} (V)	1	0.8-1.1	0.7-0.9	0.7-1.1	**0.4-0.9**
Quiescent Power (nW)	0.544	3.2	0.24	1.05	**0.802**
Peak Efficiency (%)	53	87	92	78	**93**
Dynamic Range ($P_{LOAD,\ MAX}$ / $P_{LOAD,\ MIN}$)	0.544-4nW (7.4)	10nW–1µW* (1×10^2)	0.4nW-0.8mW (2×10^6)	0.12-160nW (1.3×10^3)	**0.5nW-2.75mW (5.5×10^6)**
Dynamic Range with η > 80%	N/A	40nW-1µW*	0.9nW-0.8mW*	N/A	**4.3nW-2.75mW**
Settling Time @ ΔI_{LOAD}	>40s@N/R*	N/A	2ms@0.4mA*	N/A	**0.2ms@1mA**
Fast DVFS (T_{UP}/ T_{DOWN})	No	No	No	No	**Yes (6µs/10.76µs†)**

*Observed from the waveform
†For a 50mV reference-tracking step

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